Design of a Central Office for an ISDN System

by

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CHAPTER 1. INTRODUCTION

Rapid advances in computer and communication technologies have necessitated the integration of voice, data and video text services. The integration of these services has led to the development of ISDN.

Definition of ISDN: An ISDN is a network in general evolving from a telephony Integrated Data Network (IDN), that provides end to end digital connectivity to support a wide range of services, including voice and nonvoice services, to which users have access by a limited set of standard multi-purpose user network interfaces [1].

In order to have a central control over all the information that is passed between users, we need to have a Central Office. A complete design of a Central Office is done at the computer systems research laboratory at Iowa State University. The broad outline of how a Central Office fits into the ISDN environment is given in Figure 1.1.

The terminal equipment (TE) can be a

- digital telephone
- personal computer connected through a RS 232 interface.

The network termination (NT1) is responsible for

- Line transmission termination
- Line maintenance and performance monitoring

- Timing
- Power transfer
- Some multiplexing functions
- Termination of T interface functions.

The network termination 2 (NT2) is responsible for

- Protocol handling
- Switching and concentration functions
- Interface functions to the S and T interface
- Higher levels of multiplexing

The S, T and U reference points are shown in the Figure 1.1.

The S interface separates the user terminal equipment from the network functions of the terminal.

The T interface separates the network provider's equipment from the user equipment.

The U interface specifies the transmission method for the basic rate information transfer between the ISDN and the subscriber's premises.

In order to understand how information is passed between these interfaces we will discuss the channel arrangement and the functions of these channels in an ISDN system.

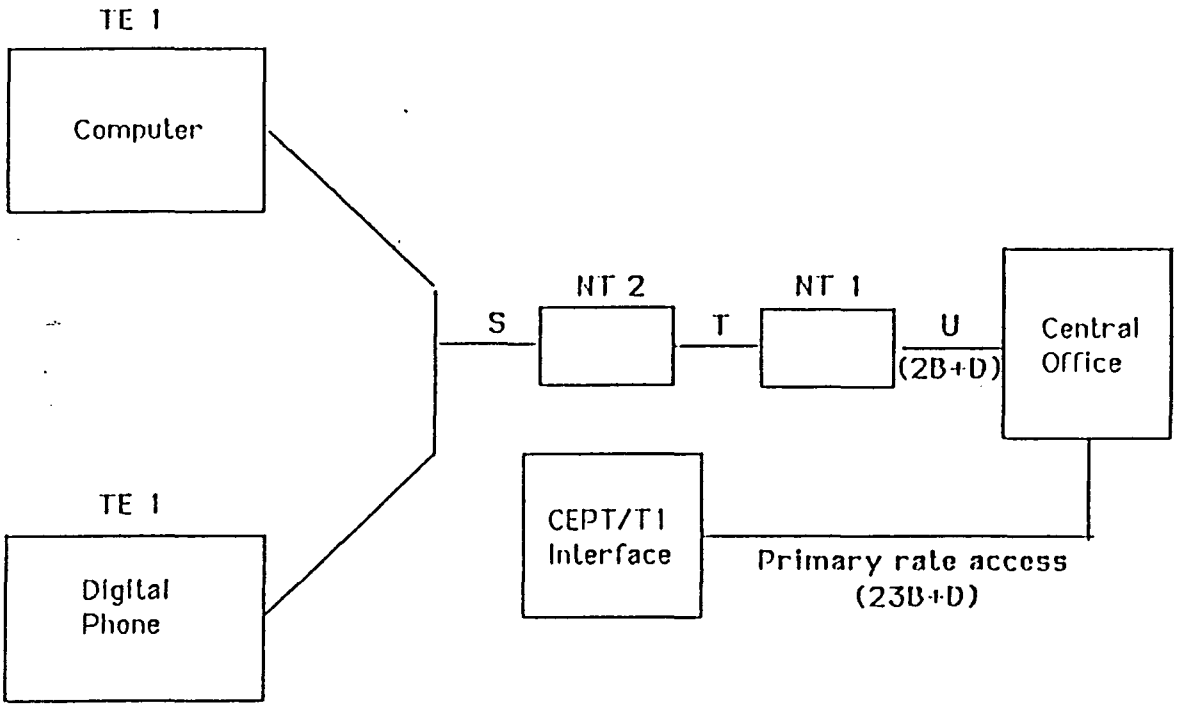

Figure 1.1: The Central Office in the ISDN environment

Channel Arrangement

The interfaces between the ISDN user and the Central Office is used to carry a number of communication channels. The transmission structure of such an interface is made up of

- B channel which carries 64 Kbps
- D channel which carries 16 Kbps
- C channel which carries 8 or 16 Kbps.

Channel Functions

The B channel is the basic user channel and is used to carry one of the following types of traffic:

- PCM encoded digital voice.
- Digital data for circuit switched or packet switched application.

The D channel is used to carry

- Signaling information
- Low speed data

The channels are grouped into the basic channel structure and the primary channel structure as shown in Figure 1.2. The basic channel structure consists of two full duplex 64 Kbps B channels and one full duplex 16 Kbps D channel. The total bit

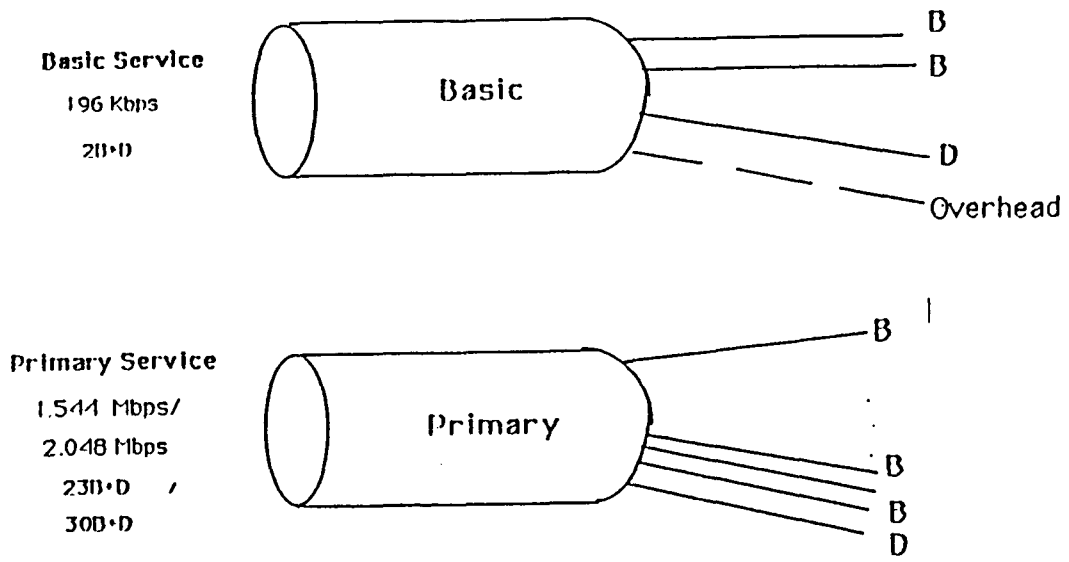

Figure 1.2: ISDN channel structures

rate is 144 Kbps but the framing, synchronization and other overhead bits bring the total bit rate to 196 Kbps on the basic access link.

The primary channel structure in North America is 23 B channels and 1 D channel corresponding to 1.544 Mbps T1 transmission facility, and in Europe is 30 B channels and 1 D channel corresponding to 2.048 Mbps CEPT transmission facility.

ISDN Layered Architecture

The development of standards for ISDN includes the development of protocols for interaction between ISDN users and the network and for interaction between different ISDN users [2]. Hence it is desirable to fit these standards into the already existing OSI framework. The Figure 1.3 suggests a relationship between OSI and

The network access is concerned only with layers 1 to 3.

Layer 1 is the physical layer which is concerned with the transmission of bits. The functions of this layer are defined in the CCITT I.430 and I.431 recommendations.

Layer 2 is the data link layer which connects the B and D channel information. The data link layer sends the D channel information to layer 3 and performs error control on the data coming from the lower layer. The functions of this layer are defined by the CCITT Q.921 recommendations.

Layer 3 is the network layer which processes the D channel information which is received in the packeted form. The functions of this layer are defined by the CCITT Q.931 recommendations.

Method

In the design and development of the Central Office at the computer systems research laboratory, an ISDN environment was simulated using the Mitel's ISDN Express card, which provides the S interface in 2B+D basic channel service [3]. A primary rate interface card, which provides the 23B+D rate service may be later used for testing and actual transmission of 23B+D channel service to and from this Central Office.

Organization of Thesis

The second chapter describes the design of the Central Office. It contains information on the MT8972 Digital Network Interface Circuit, the MT8952 High Level Data Link Controller, the MT8980 Digital Crosspoint Switch, the MH89760 Digital Trunk Interface, the MH89761 Digital Trunk Transmit Equalizer, and the MT8940

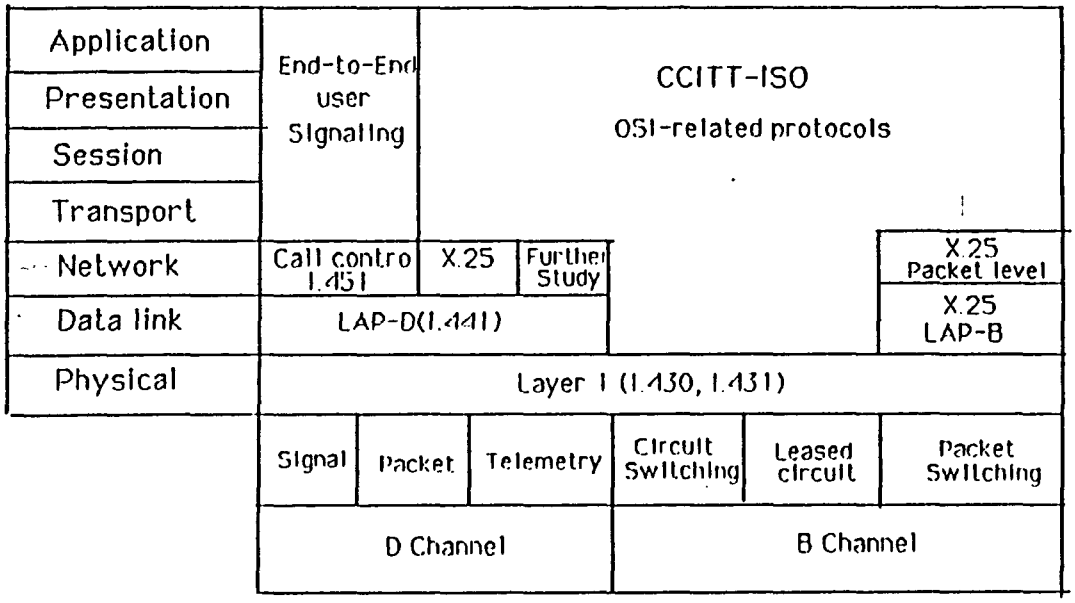

Figure 1.3: Relationship between OSI and ISDN layered architecture

Digital Phase Locked Loop used in the design of the Central Office. The last section of the second chapter describes the microprocessor interfacing with the HDLC controller. The design of the primary rate interface card is described in Chapter 3. The last chapter shows the conclusions of this research followed by the Bibliography.

CHAPTER 2. DESIGN OF CENTRAL OFFICE

The design of Central Office involves the Digital Network Interface Circuit, the HDLC protocol controller, the Digital cross point switch, the Digital trunk interface circuit and the Digital phase locked loop circuit, each of which is described in the following sections.

Digital Network Interface Circuit

The MT8972 is a device capable of providing high speed, full duplex digital transmission up to 160 Kbps over a twisted pair. In the ISDN, the DNIC is ideal for providing the interface at the U reference point. The device supports 2B+D channel format. The DNIC uses the echo cancellation technique and transfers data in 2B+D format compatible to the ISDN basic rate [4].

On the Central Office side we have the MT8972 DNIC daisy chained with three other DNICs together forming the digital line interface section as shown in Figure 2.1. The first MT8972 in the chain receives the framing signal from the system and generates a delayed framing signal for the second MT8972. Each subsequent MT8972 in the chain accepts the framing signal output by the previous MT8972 and generates a delayed signal from it. In this design data are transmitted down the lines from channels on the DSTi input stream and data from the lines are output on channels

on the DSTo output stream. The MT8972s are controlled and monitored on the channels on the CSTi and CSTo streams.

This digital line section provides 2B+D, 160 Kbit bidirectional communication over a single twisted pair wiring. The MT8972 converts the 160 Kbit line signal into the ST BUS format where it can be manipulated by the MT8980 Digital Cross point switch. The data received from the MT8972 are then transferred to the D-channel processor by the switch matrix as shown in Figure 2.2. The D-channel processor converts the 2B+D format used on the 160 Kbit digital line into the 23B+D format used on the T1 link. To control and monitor the MT8972s and the T1 interface, the switch matrix operates some of its input and output streams in the message mode. This enables the system to control all of its functions of the MT8972s and the T1 interface through the control ST-BUS points CSTo and CSTi.

Clock synchronization is done by the MT8940. The PLL 2 of the MT8940 Digital Phase Locked Loop circuit generates the ST-BUS clocks that are synchronized to the extracted 8 Khz output from the T1 interface. PLL 1 generates the transmit T1 clock synchronized to the ST-BUS clocks, which are synchronized to the extracted T1 clock. This scheme will allow the system to operate in loop timed mode.

With appropriate multiplexing, a single D-channel processor can handle all four 2B+D interfaces. The four MT8972s will be used in the Master, Digital Network(DN), Single port mode. The MT8972s provide a bidirectional interface between the DV(Data/Voice) port and a full duplex line operating at 160 Kbps over a single pair of twisted wires. When the MT8972 is operated in the Single port mode, all the data and control information appears on the DV port and the CD port are disabled.

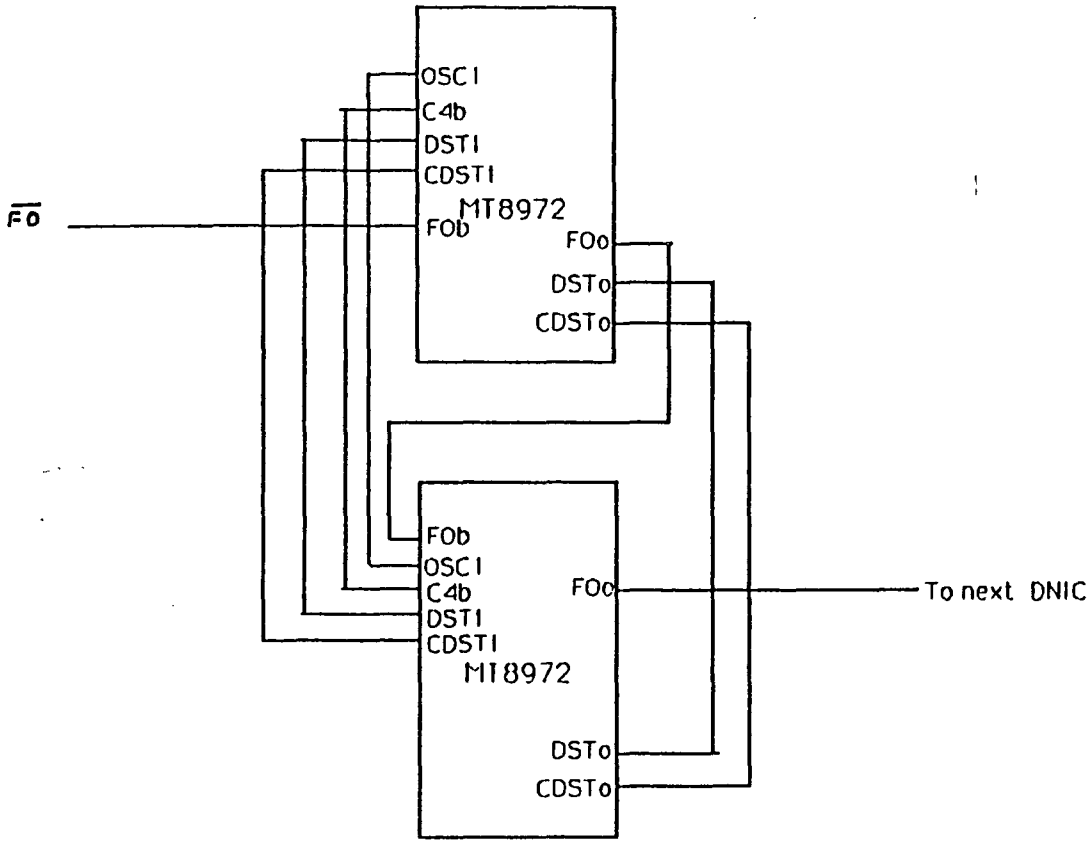

Figure 2.1: Digital line card

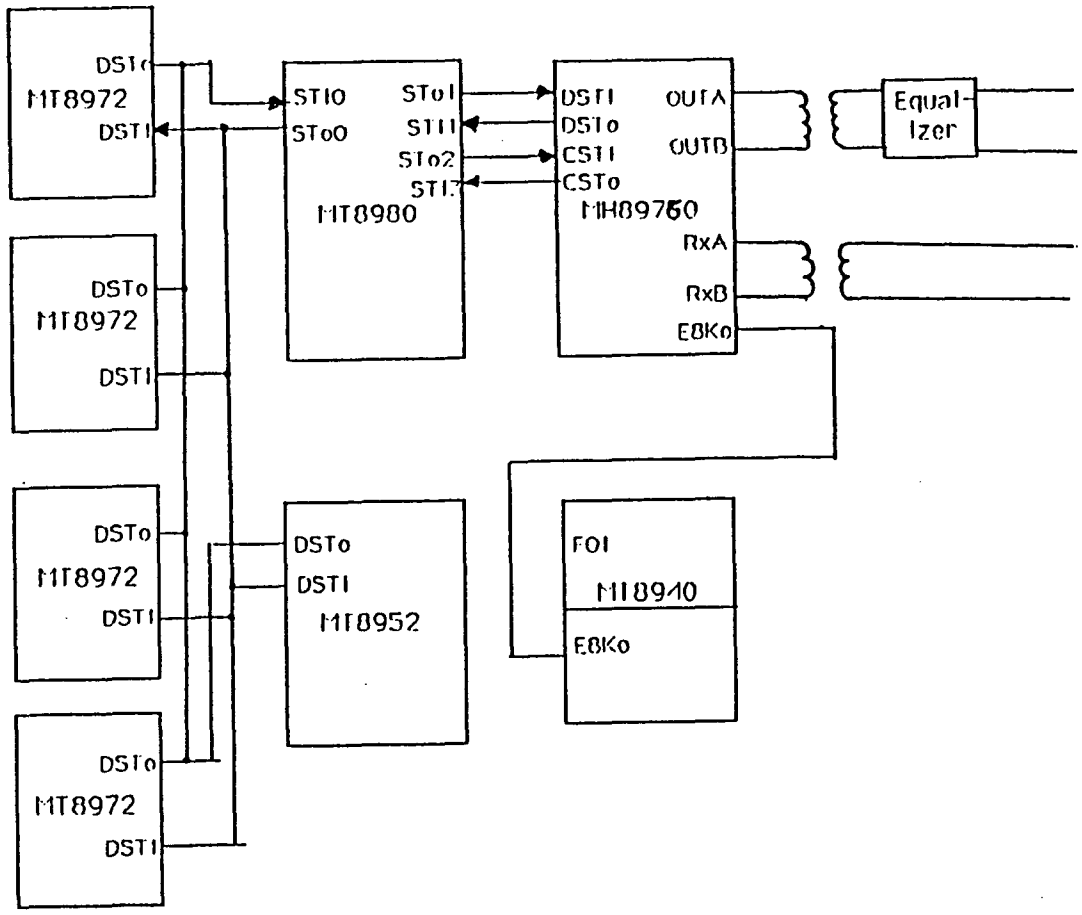

Figure 2.2: ISDN voice data channel bank

Ports of the DNIC MT8972

The DNIC has three serial ports.

- DV port [CDSTi/o]
- Line port [Lin and Lout]
- CD port [Control/data]

The data received on the line are made up of information from the DV and CD ports. The DNIC must combine the information received from both these ports and put them on the line. At the same time the data received from the line must be split into various channels and directed to the proper ports.

The DNIC has various modes of operation which can be selected through the mode select pins MS0-2. The two major modes of operation are the Modem (MOD) mode and the Digital Network (DN) mode. In the DN mode, the CD and DV ports are standard ST-BUS and in the MOD mode they are transparent to the serial data stream. Other modes are Master (MAS) and Slave (SLV) modes where the time base and frame synchronization are external (in the case of Master) and extracted from the line (in the case of slave).

There are also the Dual and Single port modes where both the DV and CD ports are active (DUAL) or where the CD port is inactive (Single).

DV Port

The DV port transfers data or PCM encoded voice from the line according to the particular mode selected by the mode select pins. The MOD/DN or Dual/Single

mode can be used in the DV port configuration. In the DN mode, the DV port operates as an ST-BUS [5] at 2.048 Mbps with 32, 8-bit channels per frame as shown in Figure 2.3. When the Dual port mode is used in DV, the C and D channels are passed through the CD port and the B1 and B2 are passed through the DV port.

At 160 Kbps two channels are used, that is, channel 1 and channel 16 to carry B1 and B2 channels, respectively as shown in Figure 2.4. When a single port mode is used in DV, channels B1 and B2, C and D are all passed via the DV port and the CD port is disabled.

CD Port

The CD Port is a serial bidirectional port used only in Dual port mode. It is composed of the C and D channels. The C channel is used for transferring control and status information between the DNIC and the system. The D channel is used for sending and receiving signaling information between the line and the system.

In DN/Dual mode, the DNIC receives a C channel on the CDSTi while transmitting a C channel on CDSTo. Fifteen channel times later, a D channel is received on the CDSTi and transmitted on CDSTo. In the MOD mode the CD port is a serial bit stream at the bit rate selected.

Line Port

The line interface is made up of L_{in} and L_{out} with the L_{out} driving the transmit signal onto the line and the L_{in} receiving the composite transmit and receive signal from the line. The line code used in the DNIC is bi-phase and is shown in the Figure 2.5. The scrambled NRZ data are first differentially encoded and then

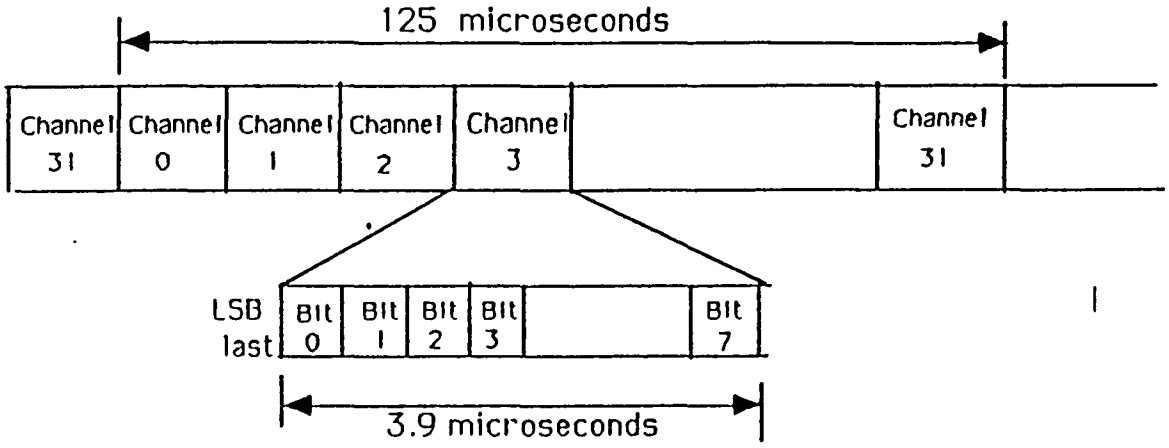

Figure 2.3: ST-BUS channels

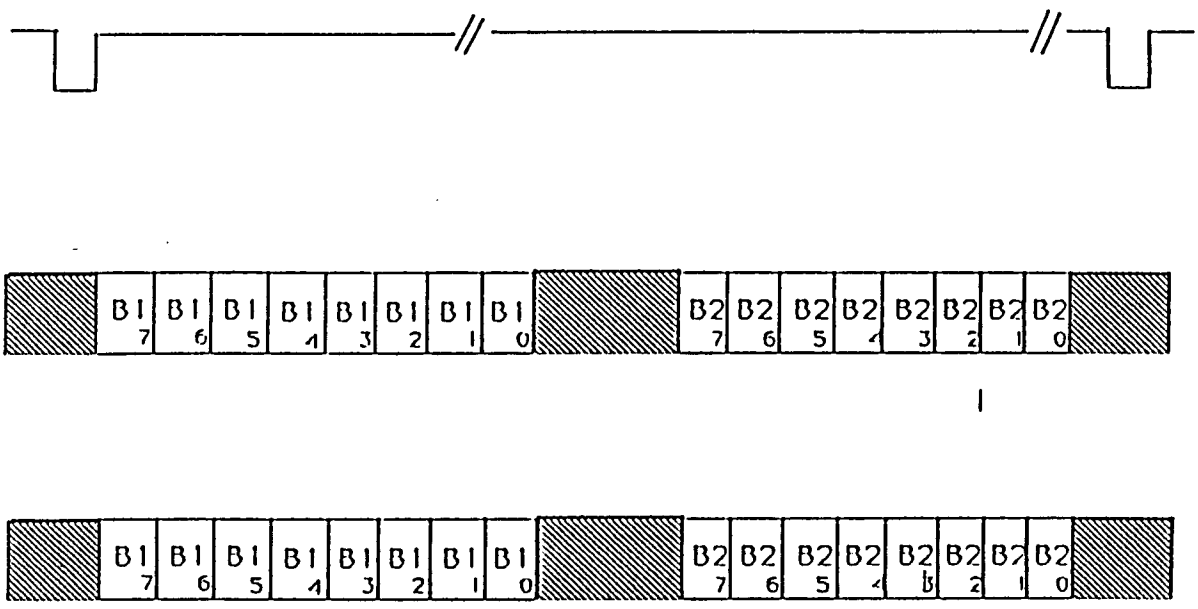

Figure 2.4: Channel allocation for B1 and B2 channels

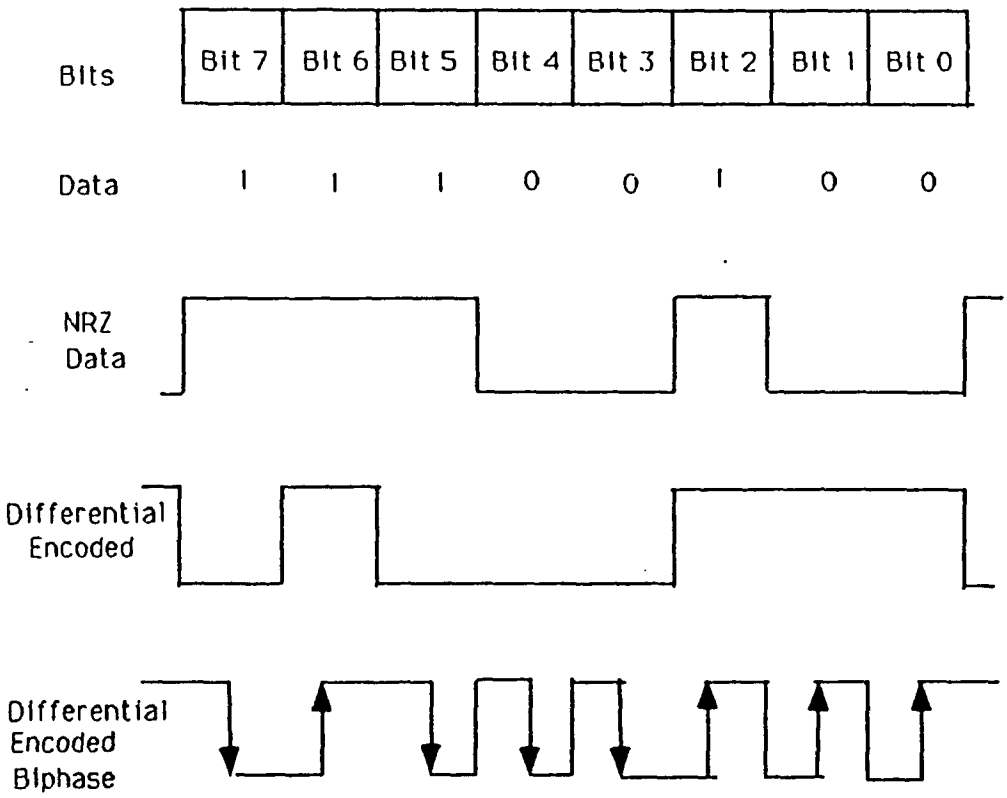

Figure 2.5: Encoding schemes in DNIC

bi-phase encoded where transitions occur midway through the bit cell with a positive going transition indicating "Logic 1" and a negative going transition indicating "Logic 0". The signal is then passed through a bandpass filter onto a line driver where it is made available to be put onto the line biased at V_{bias}.

L_{out} is connected to the coupling transformer through the resistor R2 and capacitors C2 and C2́ to match the line characteristic impedance. C1 is provided to properly bias the received line signal for the L_{in} input. A 2:1 coupling transformer is used to couple to the line with a secondary center tap for optional power feed. Refer to Figure 2.6 for a typical connection diagram in MAS/DN mode.

Clock and Synchronization

The transmit and receive control block generates all the clocks for the transmit and receive functions of the MT8972 and controls the entire chip according to the control register. The basic clock source is a 16.388 Mhz oscillator. This is used as an input to the MT8940 DPLL which provides all the ST-BUS timing signals except the C10 signal as shown in Figure 2.7. The C10 signal is generated by the phase locked loop formed by the 74LS86, 74LS624 and 74LS163. The C10 clock is the output of the 74LS624 Voltage Controlled Oscillator. This is input to the 74LS163 counter which is synchronously reset to zero after it reaches a count of four giving an output which is a 10.24 Mhz input divided by 5. This 2.048 Mhz output is compared to the C2 clock generated by the MT8940 using the 74LS86 ExOR chip. As the C2 signal slows down, the overlap between the C2 signal and the C10 signal increases causing the output of the ExOR to spend more time low. This reduces the input voltage on the 74LS624 and so causes C10 to slow down. The PLL was found to lock when the

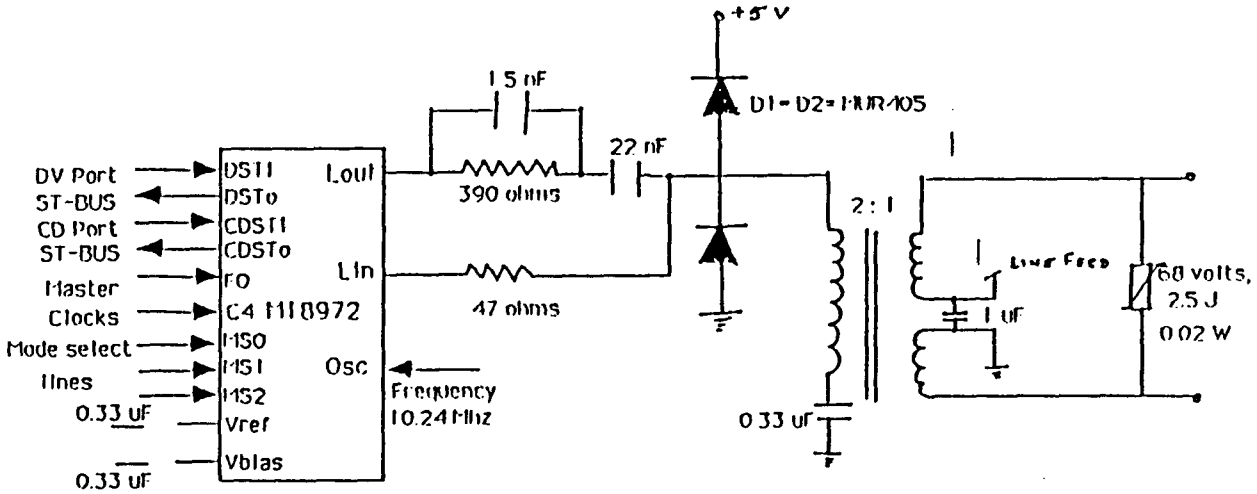

Figure 2.6: Typical Connection Diagram in MAS/DN mode

period of C2 was between 400 ns and 600 ns.

In order that more than one DNIC may be connected to the same CD and DV ports, a $\overline{FOo}$ signal is generated which signals the next device in a daisy chain that its channel times are now active. In this arrangement only the first DNIC in the chain receives the system $\overline{FOo}$ with the devices following it receiving its predecessor's $\overline{FOo}$.

Description of the HDLC Protocol Controller

The MT8952 HDLC controller handles the data as per the protocol defined in X.25 (level 2) recommendations of the CCITT. It transmits and receives the packeted data serially in the format shown in the Table 2.1. The flag is a unique pattern of 8-bits defining the frame boundary. The data field refers to the address, control and information fields defined in the CCITT recommendations [6].

The transmitter calculates the frame check sequence (FCS) on all the bits of the data field and transmits them after the data field and before the end flag. The receiver performs a similar computation on all the bits of the received data and the FCS fields. The HDLC Protocol controller MT8952 has two ports.

- Serial Port
- Parallel Microprocessor Port

The serial port transmits and receives formatted data packets on selected time slots in the ST-BUS format or it can use the enable signals $\overline{TxCEN}$ and $\overline{RxCEN}$, transmit or receive the packets at a bit rate equal to CKi clock input. The microprocessor port allows parallel data transfers between the protocol controller and the microprocessor.

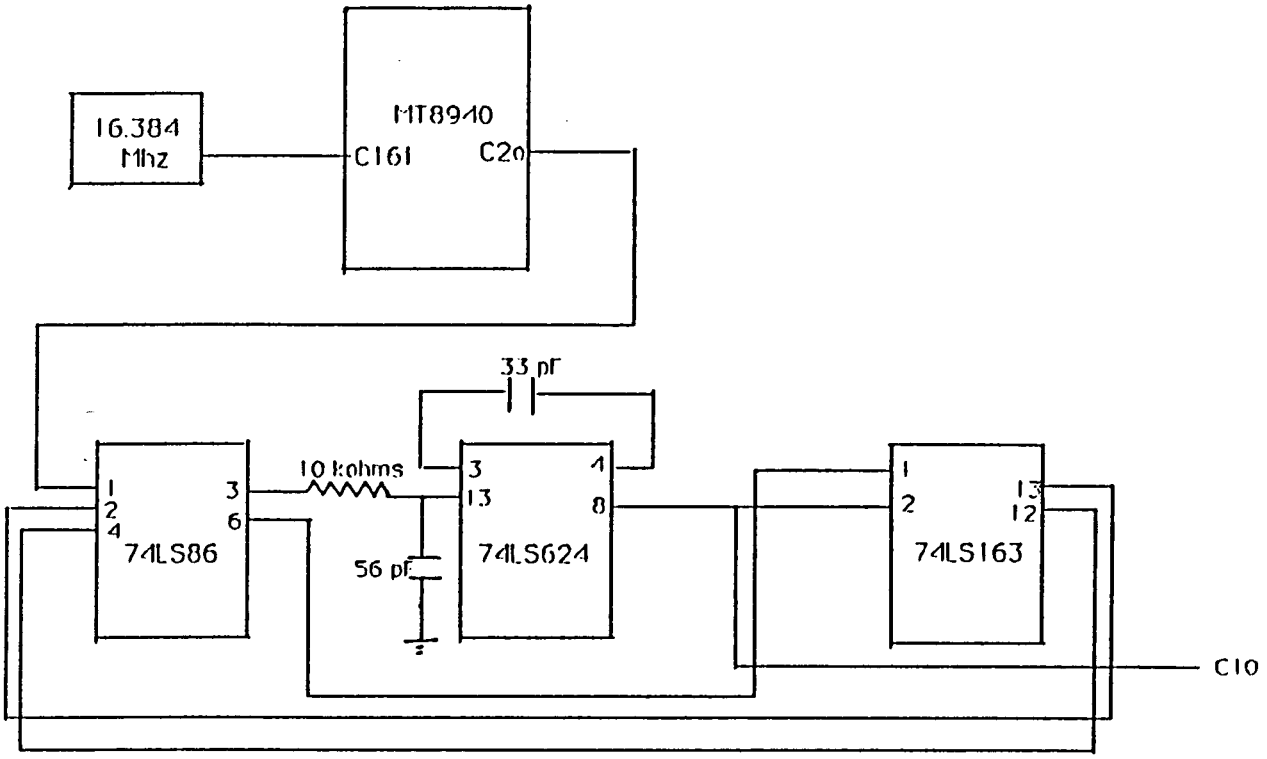

Figure 2.7: Generation of timing signals for MT8972 in master mode

Table 2.1: Data Format

Flag	Data field	FCS	Flag
1 byte	n bytes	2 bytes	1 byte

The information supplied to the Digital line circuit discussed in the previous section is done using the HDLC format for error free communication and is implemented using a Shared HDLC D channel interface using the Digital Cross point switch.

Shared HDLC Resource

In this scheme a single HDLC protocol controller is time shared between several digital line circuits as shown in the Figure 2.8. The time sharing is accomplished using the MT8980 Digital Cross-point switch.

Under the control of a microprocessor the MT8980 is used to connect the MT8952, in succession, to each DNIC's D channel at a predetermined regular interval. The B1 and B2 channels arrive at the line card at STi1 and terminate at the digital switch link STi1 where they are routed to STo2. The D channel information originating at the MT8952 arrives at the digital switch link STi3 on channel 0. This is also routed to STo2 and into the channel corresponding to the line circuit selected to receive the packet [7].

The C channels used to control the DNICs can be accessed from the parallel port of the digital switch by putting channels 1, 5, 9, 13, 17, 21, 25, 29 of link STo2 into the message mode. This combines the C channel information with the B1, B2 and D channels at the composite STo2 output link. When accessing the DNIC registers from the Digital switch, the DNIC registers bit assignments are reversed.

On the receive side, the B1 and B2 channels arriving at the Digital switch input

link STi2 from the line circuits are routed to STo1 and leave the card edge at STo1. The D channel from the selected receive line circuit is routed to channel 0 of STo3 so that the MT8952 may receive it. The digital switch data memory can be used to read the C channel status from the STi2 channels. Each DNIC D channel is active in the first time slot relative to its received frame pulse

This method employs a polling scheme using the various link states of the HDLC protocol controller and the GO-AHEAD (GA) sequence of the MT8952. Normally the incoming and the outgoing D channel links will be in an idle state [8].

If the microprocessor wishes to transmit a packet of information to a peripheral unit it simply connects channel 0 at the Digital switch STi3 to the channel at STo2 corresponding to the desired peripheral. The microprocessor then loads the message into the MT8952 transmit FIFO in the normal manner. When transmission is complete, the channel at STo2 is returned to an idle state.

If the microprocessor is receiving messages then the digital switch under the microprocessor control will sequentially connect the HDLC's receiver to each DNIC's incoming D-channel.

Description of the Digital Cross Point Switch

The MT8980 is a VLSI C-MOS device used for switching PCM encoded voice or data under microprocessor control in the Central Office. It provides simultaneous connections of up to 256, 64 Kbps channels. The MT8980 can switch data from the channels on the ST-BUS inputs to channels on ST-BUS outputs and simultaneously allow its controlling microprocessor to read channels on ST-BUS inputs or write on ST-BUS outputs (Message Mode).

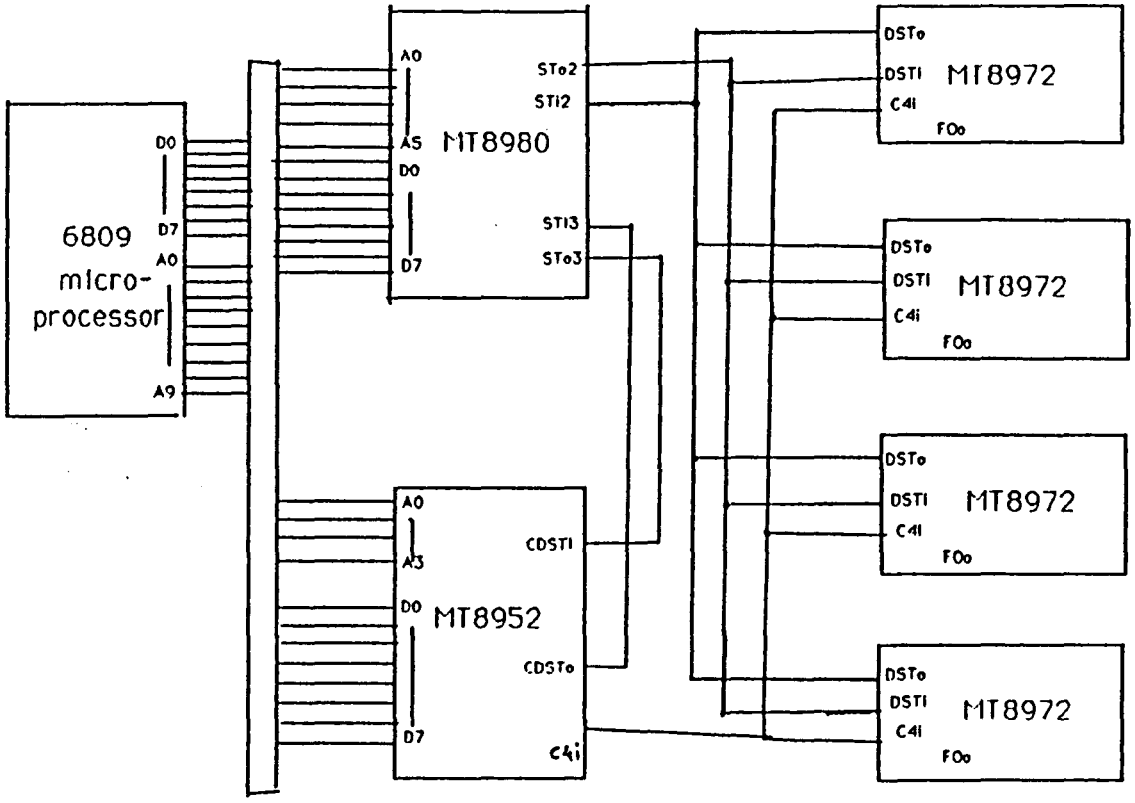

Figure 2.8: Shared HDLC D channel interface

Hardware Description

Serial data at 2048 Kbps are received at the 8 ST-BUS inputs (STi0-STi7) and the serial data are transmitted at the 8 ST-BUS outputs (STo0-STo7). Each serial data input contains 32- channels of digital data, each channel containing an 8- bit word. This serial input word is converted into parallel data and stored in the 256 x 8 data memory. Locations in the data memory are associated with particular channels on particular ST-BUS input streams. These locations can be read by the microprocessor which controls the chip [9]. Locations in the connection memory, which are split into high and low parts, are associated with particular ST-BUS output streams. When a channel is due to be transmitted on the ST-BUS output the data for the channel can be either switched from a ST-BUS input or it can originate from the microprocessor. If the data are switched from the inputs, then the contents of the connection memory low location associated with the output channel is used to address the data memory. This address corresponds to the channel on the ST-BUS stream on which the data for switching arrived. But if the data for the output channel originates from the microprocessor (Message Mode), then the contents of the connection memory low location associated with the output channel are output directly.

Software Description

The address lines on the control interface give access to the control register directly or, depending on the contents of the control register, to the HIGH or LOW sections of the connection memory or to the data memory. If address line A5 is low,

Table 2.2: Address Memory Map

A5	A4	A3	A2	A1	A0	Hex addr	Location
0	x	x	x	x	x	00-1F	control register
1	0	0	0	0	0	20	Channel 0
1	0	0	0	0	1	21	Channel 1
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
1	1	1	1	1	1	3F	Channel 31

then the control register is addressed but if A5 is high, then the address lines A0-A4 select the memory location as per the Table 2.2.

Microprocessor Interfacing to the MT8980

The microprocessor port consists of a data bus for information transfer, an address bus, a chip enable, two signals for synchronizing microprocessor bus transfers and a transfer direction control signal.

The data bus is 8-bits wide and carries control information for the MT8980 from the microprocessor. The address bits A0-A5 determine which of the individual locations are accessed. The chip select is the chip enable. If this pin is high no access to the MT8980 is possible. The data strobe signal and the data acknowledge signal perform transfer synchronization. The Read/Write signal determines the direction of information flow. When this signal is high, data are read from the MT8980 by the microprocessor. When this signal is low data are written to the MT8980 by the microprocessor [10].

Description of Digital Trunk Interface and Transmit Equalizer

The MH89760 is a complete interface to a bidirectional T1 link. The system side of this is made up of ST-BUS inputs and outputs, CSTi/o and DSTi/o signals. The DS1 line side of the device is made up of the split phase inputs (RxT and RxR) and outputs (OUTA and OUTB) that can be connected to line coupling transformers. Data for transmission on the line are clocked serially into the device at the DSTi pin. The DSTi pin accepts a 32-channel TDM ST-BUS stream. Data are clocked in with the falling edge of the C2i clock. The ST-BUS frame boundaries are defined by the frame pulse applied at the FOi pin. Only 24 of the available 32-channels on the ST-BUS stream are actually transmitted on the DS1 side. The unused 8 channels are ignored. Data received from the DS1 line are clocked out of the device in a similar manner at the DSTo pin. Only 24 of the 32-channels contain information from the DS1 line. All control and monitoring of the device is accomplished through two ST-BUS serial control inputs and one serial control output. CSTi0 accepts an ST-BUS serial stream which contains the 24 per channel control words and two master control words.

Programmable Features

The main features in the device are programmed through the two master control words which occupy channels 15 and 31 in the control ST-BUS input stream 0 which is the CSTi0 pin. These two eight-bit words are used to

- Select the different operating modes.
- Activate the features that are needed in a certain application.

- Turn on in-service alarms, etc.

Clock and Framing Signals

The MH89760 has a built-in clock extraction circuit which creates 1.544 Mhz clock synchronized with the received DS1 signal. This clock is used internally by the MH89760 to clock in data received on the RxD, $\overline{RxA}$ and $\overline{RxB}$. It is also output at the E1.5o pin for tuning the circuit during initial setup. The frequency of this extracted clock is controlled by a 43 μH to 48.5 μH external tunable inductor connected between L_a and L_b pins. The extracted clock is divided internally by 193 and aligned with the received DS1 frame. The resulting 8-Khz signal is output at the E8ko pin and can be used to phase lock the local system C2 and the transmit C1.5 clocks to the extracted clocks. The MH89760 requires three clock signals which have to be generated externally as follows.

- The ST-BUS interface requires a 2.048 Mhz signal which is applied at the C2i pin and an 8-Khz framing signal applied at the $\overline{FOi}$ pin.

- The framing signal is used to delimit individual ST-bus frames.

- The transmit side of the DS1 interface requires a 1.544 Mhz clock applied at the C1.5i. The C1.5 and C2 clocks must be phase locked.

In synchronous operation the slave end must have its C2 and the C1.5 clocks phase locked to the extracted clock.

Line Transmitter

The transmit line interface is made up of two open collector drivers (OUTA and OUTB) that can be coupled to the line with a center tap pulse transformer [11]. The capacitor and the inductor on the center tap transformer will suppress the transients in the 12 volts supply. The series RLC circuit shapes the pulse to meet the CCITT pulse templates.

To complete the interfaces to the transmit line, a pre-equalizer and line impedance matching network is required. The pulse output at the transformer secondary must be pre-equalized to drive the different lengths of the cable.

Line Receiver

The bipolar receiver inputs on the device RxT and RxR are intended to be coupled to the line through a center tapped pulse transformer as shown in Figure 2.9.

Digital Trunk Transmit Equalizer

The MH89761 is a programmable transmit equalizer for use with the T1 line interface. It contains a three-setting transmit equalizer and a 6 dB pad for external loop around, with 100 ohm input and output impedances. The seven switches control the distance settings of the equalizer. Ti, Ri, Tl and Rl are the inputs and outputs of the 6 dB pad.

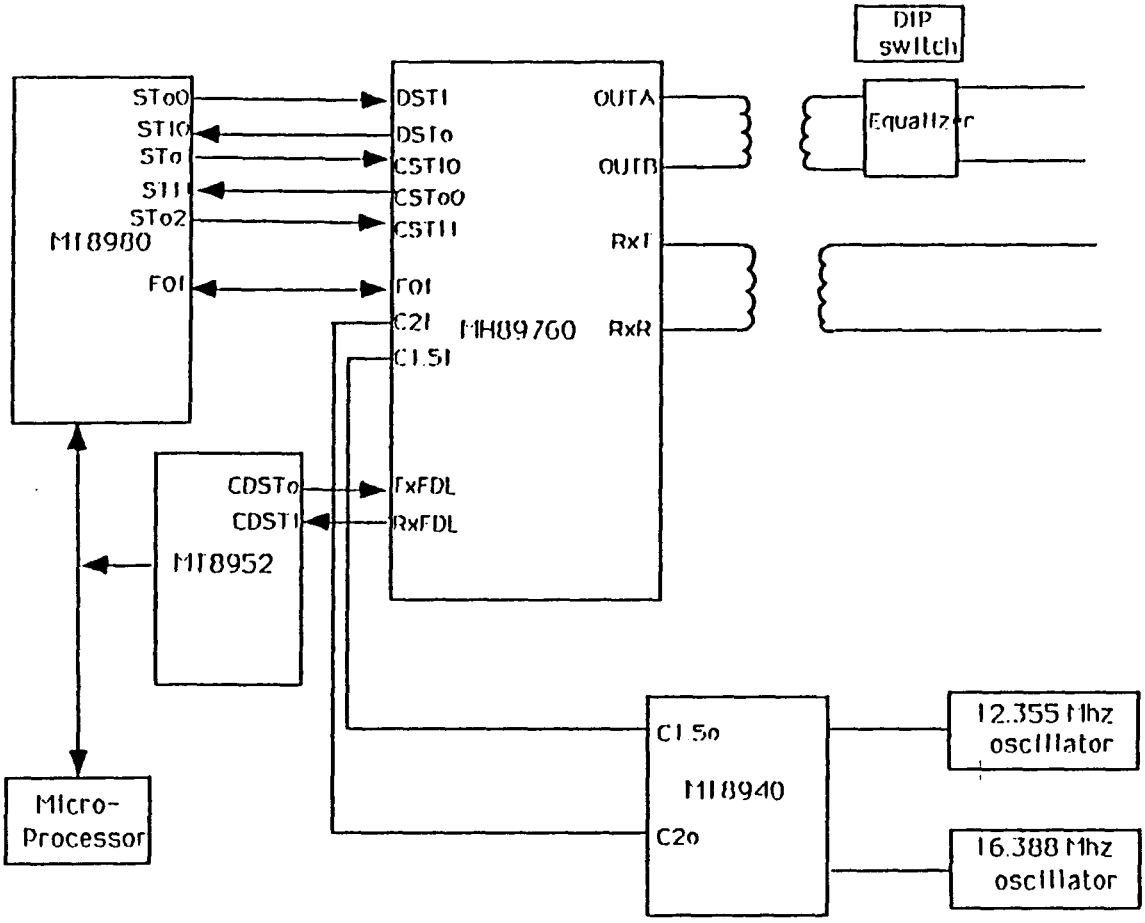

Figure 2.9: Typical Trunk Interface configuration

Description of the Digital Phase Locked Loop

The MT8940 is a Dual digital phase locked loop providing the timing and synchronization signals for the T1 transmission links and the ST-BUS [12]. The first PLL provides the T1 clock at 1.544 Mhz synchronized to the input frame pulse at 8 Khz. The second PLL provides the clock for the ST-BUS.

Principle of Operation

The principle of operation of the two DPLLs is shown in the Figure 2.10. A master clock is divided down to 8 Khz where it is compared with the 8 Khz input and depending on the output of the phase comparison the master clock frequency is corrected. The MT8940 achieves the frequency correction in both directions by using the master clock at a slightly higher frequency and dividing it unaltered or stretching its period before the division, depending on the phase comparison output. When the input frequency is higher, the unchanged master clock is divided, thus effectively speeding up the locally generated clock and eventually pulling in synchronization with the input. If the input frequency is lower than the lower replica, the period of the master clock is stretched by half a cycle, at two discrete instants in a phase sampling period, thereby introducing a total delay of one master clock period over the sampling duration and then dividing it to generate the local signal which will be in synchronization with the input [13]. Once the output is phase locked to the active edge of the input, the circuit will remain in the locked condition, as long as the input frequency is within the lock-in range of the DPLLs. The phase sampling is done once in a frame (8 Khz) and the divisions are set at 8 and 193 for the DPLL 1,

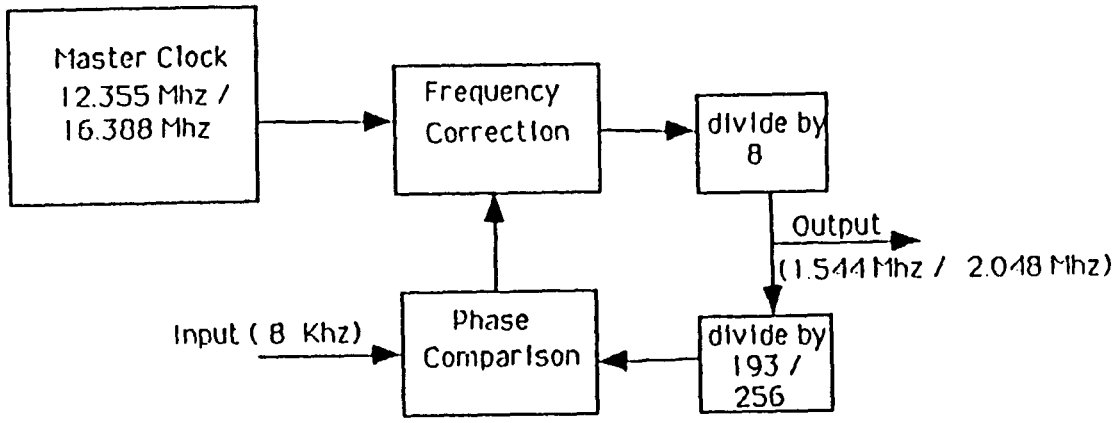

Figure 2.10: The Principle of DPLL

locks on to the falling edge of the input at 8 Khz to generate T1 (1.544 Mhz) clock. Although the phase sampling duration is the same for DPLL 2, the divisions are set at 8 and 256 to provide the ST-BUS clock at 2.048 Mhz, synchronized to the rising edge of the input signal.

Modes of Operation

The operation of the MT8940 is categorized into two types.

- Major Modes
- Minor Modes

The major modes are defined by the mode select pins MS0 and MS1. The minor modes are defined by the mode select pins MS2 and MS3 and are applicable only to

Table 2.3: Major Modes of DPLL 1

MS0	MS1	Mode of operation	Function
X	0	Normal	Provides T1 clock
0	1	Divide-1	divides the CVb input by 193
1	1	Divide-2	divides the CVb input by 256

Table 2.4: Major Modes of DPLL 2

MS0	MS1	Mode of operation
0	0	Normal
1	0	Free-run
0	1	Single clock-1
1	1	Single clock-2

DPLL 2. Table 2.3 to Table 2.5 describe the modes and the operational characteristics for DPLL 1 and 2.

Synchronization and Timing Signals for the T1 Transmission Link

An example of providing the timing signals to the MH89760 is shown in the Figure 2.11 for the slave end of the T1 transmission link.

The frame pulse output is looped back to the DPLL 1 which locks onto it to generate the T1 line clock. At the slave end of the link as shown in Figure 2.12 both the DPLLs are in "normal" mode with the DPLL 2 providing the ST-BUS timing signals locked to the 8 Khz frame pulse (E8ko) extracted from the received signal on the T1 line. The regenerated frame pulse is looped back to the DPLL 1 to provide the T1 line clock at the master end. The 12.355 Mhz and 16.388 Mhz clock sources are necessary for the DPLL 1 and DPLL 2, respectively. The uncommitted NAND gate regenerates the received signal in return to zero format as at the master end.

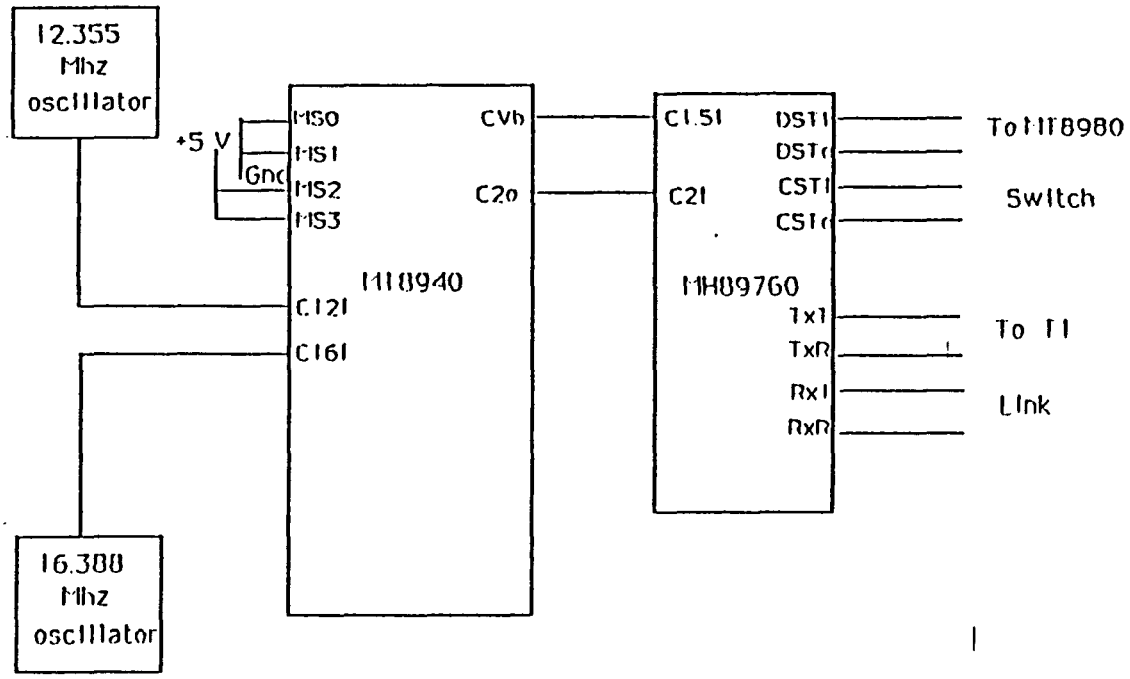

Figure 2.11: Synchronization at the slave end of the T1 transmission link

Table 2.5: Minor Modes of DPLL 2

MS2	MS3	Mode of operation
1	1	provides ST-BUS compatible 4.096 and 2.048 Mhz clocks depending on major mode selected.
0	1	provides ST-BUS compatible 4.096 and 2.048 Mhz clocks depending on major mode selected while $\overline{Fob}$ acts as input.
0	0	overrides the major mode selected and accepts properly phase related external 4.096 Mhz clock and 8 khz frame pulse to provide the ST-BUS clock at 2.048 Mhz.
1	0	overrides the major mode selected and accepts an external clock at 4.096 Mhz to provide the ST BUS clock and frame pulse at 2.048 Mhz and 8 Khz respectively.

Microprocessor Interfacing to the HDLC Controller

The MT8952 HDLC controller can be used to transmit data and/or voice over a twisted pair when it is used in combination with the MT8972 DNICs. Figure 2.12 shows one such application of the HDLC controller. The MT8952 operates in the internal timing mode with the C channel transceiver action enabled. The microprocessor loads the data or control information (D channel) in transmit FIFO which are packetized in HDLC format and shifted out serially during the selected channels of the outgoing ST-BUS (CDSTo). The channels and the number of bits per frame can be selected TC0-TC3 bits in the timing control register of the HDLC controller. Since channel 1 is reserved for C channel information and channels 2 and 3 carry B channels, the D channels information is sent on channel 0.

Similarly, the incoming packets on CDSTi are loaded into the receive FIFO after the removal of all overhead bits and checked for errors. The microprocessor will then

read the data from the receive FIFO.

The DNIC is selected to operate in the single port, master mode with the DN option enabled. The B channels B1 and B2 are shown connected directly to the DNIC. Hence these should be in the ST-BUS format enabled at appropriate time-slot.

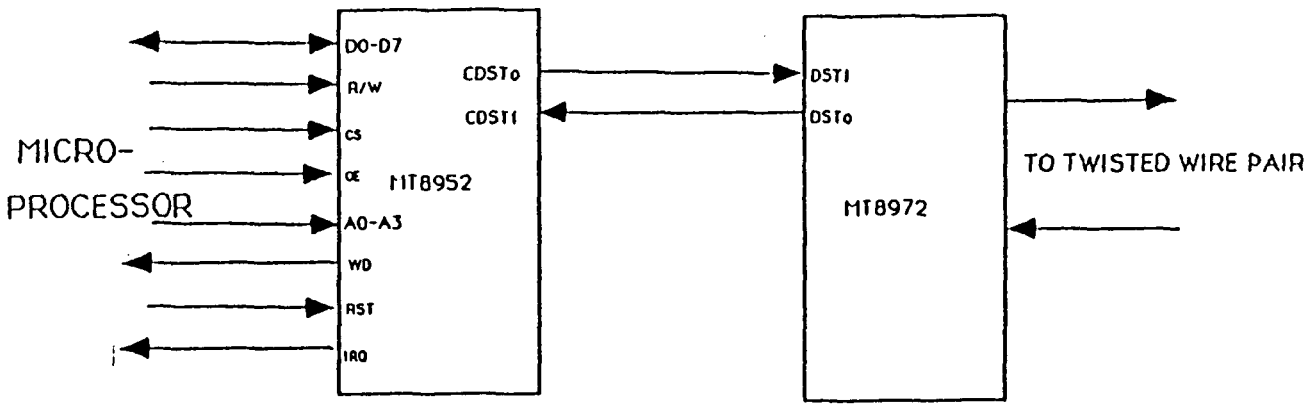

Figure 2.12: Microprocessor interfacing to the HDLC controller

CHAPTER 3. DESIGN OF PRIMARY RATE INTERFACE CIRCUIT

The ST-BUS Parallel Access Circuit

The ST-BUS Parallel Access (STPA) Circuit provides a simple interface between the ST-BUS and the parallel system environments. For interfacing parallel data and control information to the ST-BUS, such as signaling and link control for the digital trunks, the STPA provides a microprocessor access mode (Mode 1). In this mode the device provides powerful interrupt features, useful in monitoring digital trunk or line status or setting up message communication links between microprocessors.

To interface high speed data or multi-channel voice/data to the ST-BUS for switching or transmission, the STPA has a high speed synchronous access mode (Mode 2) and acts like a fast RAM. For voice storage and forward, bulk data transfer, data buffering and other similar applications, the STPA has a controller-less mode (Mode 3) in which it provides address and control signals to the parallel bus.

Modes of Operation

The three basic modes of operation are selected using two external input pins. These inputs are MMS and MS1.

- When MMS=0; Modes 2 or 3 are selected as determined by MS1.
- When MS1=1; Mode 2 is selected

- When MS1=0; Mode 3 is selected.
- When MMS=1; the device resides in Mode 1.

24/32 Channel Operation

The STPA may be configured to operate as a 32-channel or a 24- channel device. This feature is particularly useful in applications involving data access to CEPT and T1 digital trunk interfaces. When used as a data interface to the T1 trunk devices, only the first 24 consecutive RAM locations are mapped to the 24 of the 32-channels with every fourth channel beginning at channel 0, set to FF_{16}. When the STPA is operated in Mode 1, 24 and 32-channel configuration are selected using the bit D5 in the control register 1. D5=0 selects the 32-channel operation and D5=1 selects the 24 channel operation. When the STPA is operated in modes 2 or 3 the channel configuration is done using the $\overline{24}$ /32 pin.

Dual Port RAMS

Each of the three serial ST-BUS streams is interfaced to the parallel bus through a 32-byte dual port RAM. This allows parallel bus accesses to be performed asynchronously while accesses to the ST-BUS port are synchronous with the ST-BUS clock.

Mode 1: Microprocessor Peripheral Mode

In this mode the STPA acts as an asynchronous 68000 type microprocessor peripheral. All three dual port RAMs are made available and may be configured as 32- or 24-byte RAMs.

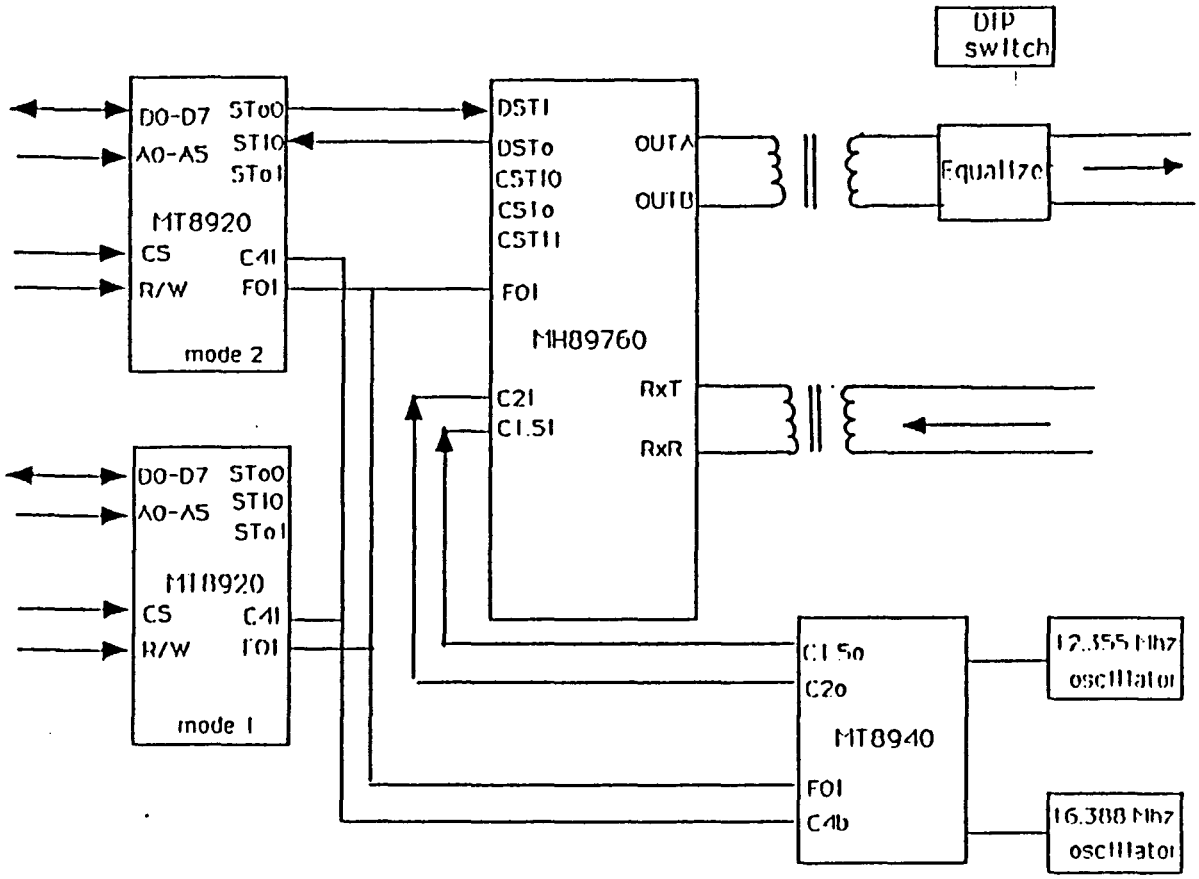

Figure 3.1: Typical Primary Rate Interface Configuration

Mode 2: Fast RAM Mode

Mode 2 acts as a high speed dual port RAM interface to the ST-BUS. Only the two transmit RAMs Tx0 and Tx1 and the receive RAM, Rx0 are active in this mode. The main feature of this mode is fast access to the dual port RAMs which enables this device to be used as a data interface to T1 and CEPT digital links. Mode 2 can also support 24- or 32-channel operation.

Mode 3: Parallel Bus Controller

In this mode the STPA outputs all necessary signals required to drive devices attached to the parallel port. Mode 3 can also operate in 24- or 32-channels.

Interfacing to the Digital Trunks

Figure 3.1 shows a typical interface for the T1 digital trunk. The MH89760 T1 trunk module is shown interfaced to a parallel bus structure using the two STPAs operating in modes 1 and 2 discussed in the previous section.

The first STPA, operating in mode 2, routes data and/or voice information between parallel telecom bus and the T1 link via the DSTi and DSTo.

The second STPA, operating in mode 1, provides access from the signaling and link control bus to the MH89760 status and control channels. All signaling and link functions can be controlled through the STPA transmit RAM's Tx0 and Tx1, while status information is read at receive RAM Rx0.

CHAPTER 4. CONCLUSIONS

The Central Office for an ISDN system was designed and built using the data and components supplied by Mitel Corporation, U.S.A. This Central Office can transmit data between four ISDN NT1 systems connected via the U interface. Data can be transmitted and received in the basic rate service 2B+D as well as the primary rate service 23B+D.

In testing this Central Office, the basic rate service was used. This was simulated using the Mitel's ISDN Express-card. The Digital cross point switch, MT8980, and the HDLC protocol controller MT8952 are tested for data and address locations in its buffer. Data are written into and read out of these components using the assembly language programming on the IBM PC.

Scope for future work: This Central Office can be further improved by providing the primary rate interface. The primary rate interface card is designed as discussed in this thesis. The MT8952 HDLC controller can drive upto eight DNICs. Since only four such DNICs are used in this design, we can have four more of the DNICs using the HDLC controller on this card. Furthermore, the MT8980 Digital cross point switch in this design uses only three of its ST-BUS inputs and outputs. Hence the remaining ST-BUS inputs and outputs can be used for switching other devices through this Digital cross point switch.

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