Design and characterization of voltage controlled oscillators using thin film resonator based filters

by

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A Thesis Submitted to the

Graduate Faculty in Partial Fulfillment of the

Requirements for the Degree of

MASTER OF SCIENCE

Department: Electrical Engineering and Computer Engineering
Major: Electrical Engineering

Iowa State University
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1989

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1. INTRODUCTION

The thin film resonator (TFR) and the filters based on TFR technology are revolutionary devices in terms of size, function, and the ability to be fully integrated along with other devices on a common substrate [1]. Recently, TFR based oscillators have been designed, constructed, and tested. Pierce oscillator circuits operating in the range of 250 to 300 MHz. have been reported on in both hybrid form [2] and monolithic form [3]. TFR based microwave filters which include the monolithic and stacked crystal filter (SCF) have also been used as the feedback network of oscillators operating in the neighborhood of 1 GHz. [4] [5]. The purpose of the research work is to investigate the design and operation of novel oscillator circuits, and to characterize the oscillators in terms of their individual components and overall closed loop performance with an emphasis on phase noise analysis.

In particular, the areas of original contribution include:

1. Applying microwave engineering techniques to the design of TFR based oscillators on microstrip.
2. Improving the means of packaging TFR based devices for use in microstrip circuits and modeling the associated parasitics.
3. Characterization of the stacked crystal filter and the optimization of its equivalent circuit model parameters.
4. Design and analysis of a voltage controlled oscillator (VCO) operating at a fundamental frequency of over 1 GHz using the SCF.

5. Design and analysis of a frequency selectable oscillator employing an overmoded filter structure.

6. Characterization of TFR based filters with respect to open loop flicker noise measurements.

The advantages of TFR technology are numerous indeed. In terms of potential space and weight savings, the monolithic TFR based circuits outperform any competing technologies. Indeed, no other means of providing reactive feedback such as quartz crystals, resonant cavities, stripline, and the like are compatible with current IC processing and offer the possibility of full integration. Even when TFR based oscillators are constructed in hybrid form, they still offer considerable savings in terms of weight and space over existing technologies.

Applications of the TFR based oscillators include a signal source that could be integrated on a common substrate with digital or analog circuitry. A VCO operating in the vicinity of 1 GHz. might see application as a temperature controlled oscillator (TCXO). The VCO would also be easily adaptable to frequency or phase modulation schemes, and results will be presented in Chapter 4 for a single frequency phase modulated carrier at 1.04 GHz to demonstrate this. The VCO may be used to phase lock to a highly stable TCXO reference source in order to improve the overall noise performance, since low frequency quartz oscillators multiplied up to 1 GHz will generally have superior noise performance close to the carrier, but are poorer than fundamental mode oscillators away from the carrier [6, p. 89].

The oscillator design examples progress from designing a simple oscillator circuit, adapting it to allow tunability, and the extension of the design to allow voltage controlled tuning. Finally the design of a selectable mode oscillator using an overmoded filter structure will be presented which is based on the design techniques employed in the preceding oscillator examples.

2. SCF MODEL OPTIMIZATION

2.1. Overview

The material related to TFR technology and the derivation of the lumped parameter model for the SCF is presented in a highly condensed form in order to provide the reader with a basic understanding of the origins of the model parameters. In the process of obtaining a circuit model that is tractable, it is assumed that the TFR devices are passive and linear. While the series stacked crystal filter, which is the subject of the optimization routine, does exhibit a high degree of symmetry, slight differences in the measurement of S_{11} and S_{22} seem to indicate that some asymmetry or nonuniformity may exist which is not accounted for in the electrical equivalent model. Noting this, and the simplifications and assumptions used in deriving the model, the electrical equivalent model should be accepted for what it is, a model whose parameters are optimized to match a measured response over a narrow range of frequencies. In the formation of the optimization file used in Touchstone [7], the fundamental relationships of the TFR device are preserved, and the variables such as the coupling coefficient and Q are restricted to a range of reasonable values as predicted theoretically and also as measured. In so doing, we obtain a model based on the Butterworth-VanDyke equivalent circuit of a resonator whose parameters are modified to match a measured response.

2.2. TFR Based Device Models

The thin film resonator is an electromechanical device which is similar in function to the familiar quartz crystal resonator. The main difference between the two is that quartz resonators are machined from a bulk material, whereas thin film resonators are fabricated by growing a piezoelectric material on top of a substrate using microelectronic processing techniques. This difference allows the fabrication of miniature resonators with fundamental frequencies much higher than those attainable in quartz which can be fabricated on a common substrate with other semiconductor devices [1]. The Butterworth-VanDyke electrical equivalent circuit commonly used to model quartz resonators may also be applied to the TFR, and is shown in Fig. 2.1.

TFR technology has been applied to the fabrication of composite devices including monolithic filters and the stacked crystal filter and overmoded stacked crystal filter. The oscillators reported on in the subsequent chapters used the stacked crystal filter as the frequency selective device.

The stacked crystal filter was demonstrated in the early 1970s by A. Ballato and T. Lukazek using two quartz resonators bonded together to accomplish a tight coupling of modes between the individual resonators [8]. Their work resulted in devices displaying a bandpass filter function below 10 MHz. The maximum frequency of stacked crystal filters made of quartz is limited by the ability to cut crystal plates thin enough to accommodate the acoustical wavelength in the material which decreases as the desired frequency increases. The TFR devices are

fabricated by growing piezoelectric films and consequently the upper frequency limits are determined by the structural integrity of the material while lower frequency limits are determined by the maximum thickness of films which can be grown [9].

The TFR based stacked crystal filter is constructed by growing layers of aluminum nitride (AlN) or zinc oxide (ZnO) and depositing layers of aluminum to create a sandwich type structure which is shown schematically in Fig. 2.2. Growing films in this manner eliminates the bonding necessary in quartz stacked crystal filters. Since the films exhibit a large lateral dimension to thickness ratio, a one dimensional analysis is justified in deriving the equivalent circuit [10]. This plane wave analysis results in the Mason equivalent circuit shown in Fig. 2.3 and is valid for the fundamental resonance mode. Assuming that the two layers of piezoelectric material are of identical thickness, and neglecting the ohmic loss of the metal layer between them, the model may be simplified to the equivalent circuit shown in Fig. 2.4. Further simplifications to the model can be made by considering its function near the fundamental frequency, and by replacing the impedance of a single resonator given by $2Z_{r1}$ with the Butterworth-VanDyke equivalent circuit from Fig. 2.1 resulting in the electrical lumped element model shown in Fig. 2.5. The C_o term is an electrical parameter which results from the capacitance across the terminals of the device as determined by the dimensions of the electrodes and the film's dielectric constant. The R_s parameter represents the loss in the filter, C_s is dependent on the C_o term by the coupling coefficient K which is also referred to as

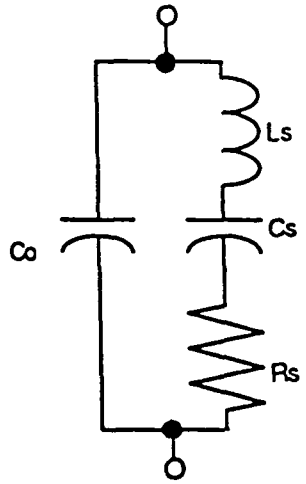

Fig. 2.1
Resonator Equivalent Ckt

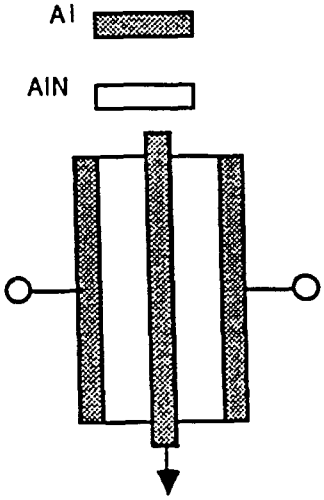

Fig. 2.2
SCF Topology

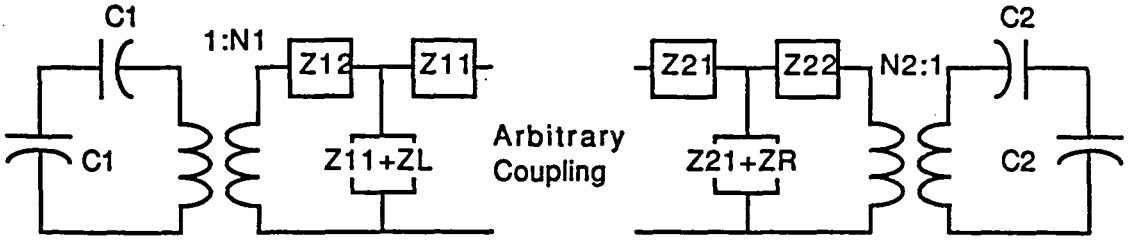

Fig. 2.3
Mason Model of SCF

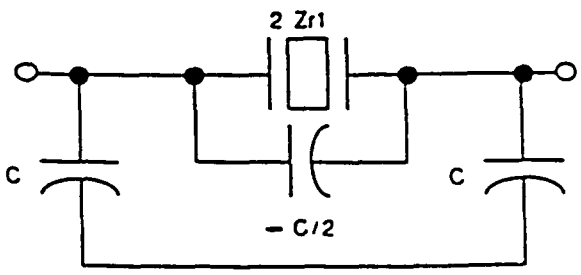

Fig. 2.4
Simplified Circuit

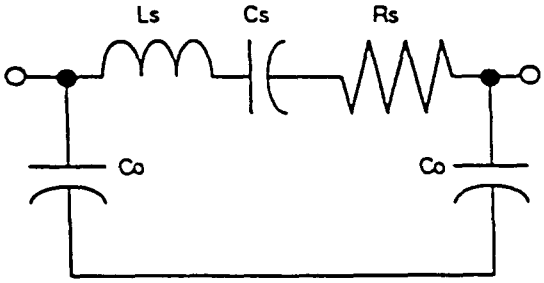

Fig. 2.5
Lumped Parameter Model

the stiffness coefficient, and the parameter L_s is the series inductance needed to resonate with C_s at f_s.

Stacked crystal filters have been fabricated in single and double section (series) configurations to achieve different passband behaviors. Theoretical curves for 1, 2, and 3 section filters are shown in Fig. 2.6 [9]. The extension of the equivalent circuit model of the single section stacked crystal filter to the multiple section stacked crystal filter is accomplished by multiplying the ABCD matrices of two filter sections together which results in the circuit shown in Fig. 2.7 for a double section SCF. The interdependence of the parameters is given in Eqs. 2.1 through 2.3 where ω_p is approximately equal to $\omega_s = 2\pi f_s$.

$$C_s = \frac{C_o}{(2K/\pi)^2} \tag{2.1}$$

$$R_s = \frac{1}{\omega_p C_o (2K/\pi)^2} \tag{2.2}$$

$$L_s = \frac{1}{\omega_s^2 C_s} \tag{2.3}$$

An actual filter's response is shown in Fig. 2.8. The first maxima occurs at the 500 MHz where the composite structure supports one half of a wavelength. The second maxima occurs at approximately 1 GHz, and is the mode which is predicted by the lumped parameter model. The responses occurring at multiple half wavelengths, although not predicted by the simplified model, may themselves be included by adding the

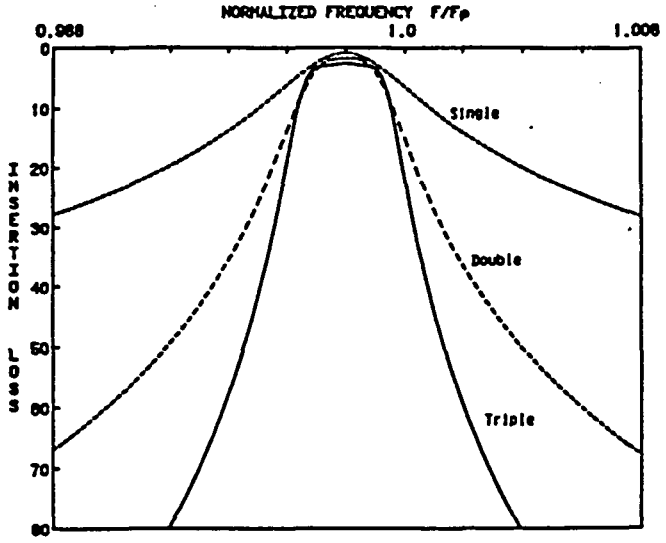

Fig. 2.6
Theoretical Response of 1, 2, and
3 Section Stacked Crystal Filters

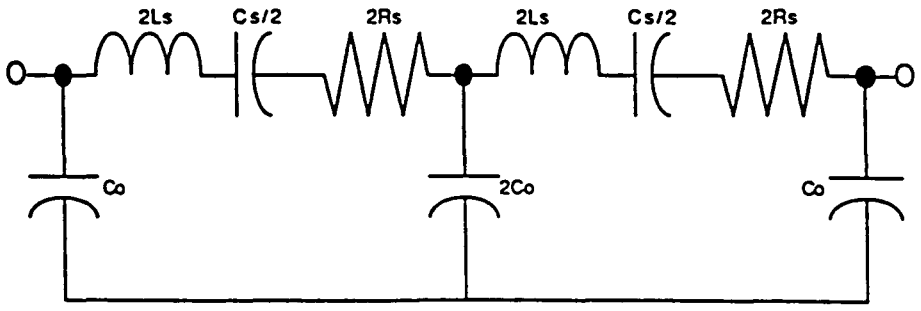

Fig. 2.7
Series SCF Equivalent Ckt

appropriate equivalent circuit models in parallel with the fundamental, although such a rigorous treatment is unnecessary when the filter is used in a fundamental mode oscillator.

Although it may not be entirely accurate from a theoretical standpoint, due to the many simplifications necessary to yield a tractable model, the lumped parameter equivalent circuit model is useful in understanding the operation and characteristics of the stacked crystal filter when it is ultimately used in an electrical circuit. Furthermore, the characterization of the filter with an electrical model is necessary when circuit analysis techniques are applied to determine the overall circuit's behavior employing the stacked crystal filter. The lumped parameter model is a necessity if a computer simulation program such as SPICE version 2G.6 is to be used in the prediction and analysis of circuits employing the stacked crystal filter [11]. In particular, SPICE was used in predicting the frequency of oscillation, output power, and harmonic content of the oscillator circuits based on the stacked crystal filter [12]. To determine the values of the circuit model elements, an optimizing routine was employed using Touchstone and the actual measured S parameters of a stacked crystal filter.

2.3. Measuring SCF S Parameters

The measured S parameters for a filter may be obtained by taking swept frequency measurements on a network analyzer. The HP8510 and HP8505 were both used to accomplish this. The HP8510 used was set up

for die probing unpackaged parts using a set of coplanar waveguide tips which maintain a characteristic impedance of 50Ω to the device under test (DUT). Provided that the analyzer is properly calibrated, and that there are no parasitics associated with the probe tips, the HP8510 is the best analyzer to characterize the embedded circuit. Swept measurements are automatically recorded and may be printed out, or the operator may interface with a controlling computer which uses a data acquisition program to record and store the swept measurements.

The oscillator circuits are built on microstrip and thus require that the filter be suitably packaged. Characterization of packaged filters is accomplished by mounting them in a microstrip test fixture that is identical to the circuit board used to construct the oscillator. A microstrip overview is given in Appendix A and a discussion of packaging techniques and the associated parasitics is presented in Appendix B. The characteristics of a packaged device are similar to the unpackaged device within the passband, but differ dramatically at the skirts of the filter. If the filter model is to include the effects of the parasitics, the HP8505 network analyzer set up with 50Ω cables and SMA type connectors is the better choice. The measurements were taken and recorded manually which is obviously a more time consuming process, but its advantage is that it allows the operator to emphasize the measured data by taking more measurements at key points. For example, a few measurements are sufficient to characterize the filter away from its passband whereas numerous measurements should be taken where the amplitude and phase of the filter is changing rapidly with respect to

frequency. Varying the frequency resolution of the measurements in this manner will result in a better set of measurement parameters for the model optimization since the Touchstone program minimizes the error over the data points and uses a straight line approximation between data points.

The basic model of the stacked crystal filter is referred to as the embedded circuit and is shown in Fig. 2.7. The embedded circuit represents the simplest two port which we can measure externally. An additional term, R_{met}, is included in series with ports 1 and 2 of the embedded circuit to account for the losses in the filter's electrodes as shown in Fig. 2.9. It is important that this parameter is treated separately from the R_s parameter since R_s is dependent on acoustic losses within the piezoelectric material and should not include any ohmic losses in the electrodes. The value of R_{met} may be calculated empirically by Eqs. 2.4a and 2.4b, where N is the number of squares, t is the thickness of the aluminum, ρ is the resistivity in $\Omega - \mu$, and $R_\square$ is the sheet resistance in ohms per square.

$$R_\square = \rho/t \tag{2.4a}$$

$$R_{met} = R_\square \times N \tag{2.4b}$$

Some typical values are; $\rho = .03$, $N = 9$, and $t = .24\mu$. This gives a value of 1.13Ω for R_{met}. The skin depth δ for aluminum at 1 GHz is approximately 2.6μ which is greater than the thickness of the electrode. Since $\delta > t$, the current distribution within the aluminum should be relatively constant, so that the skin effect may be neglected.

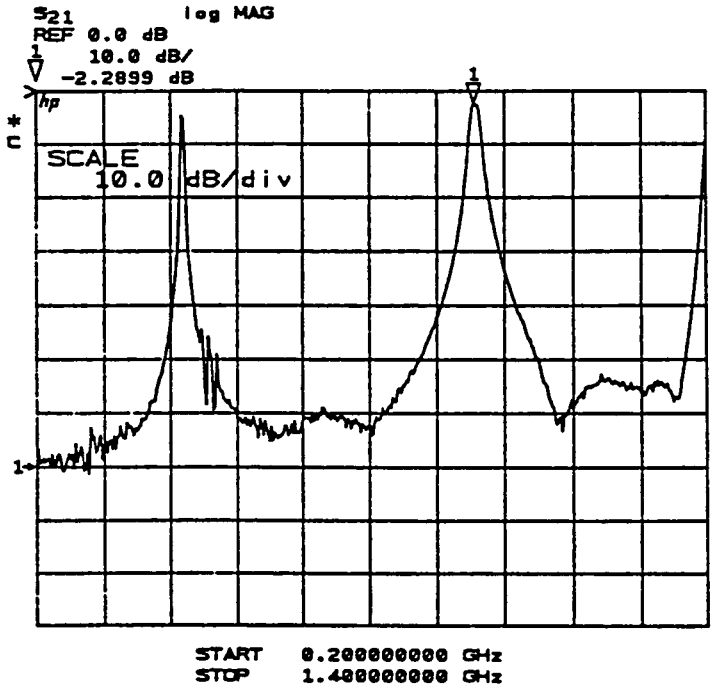

Fig. 2.8
SCF Actual Response

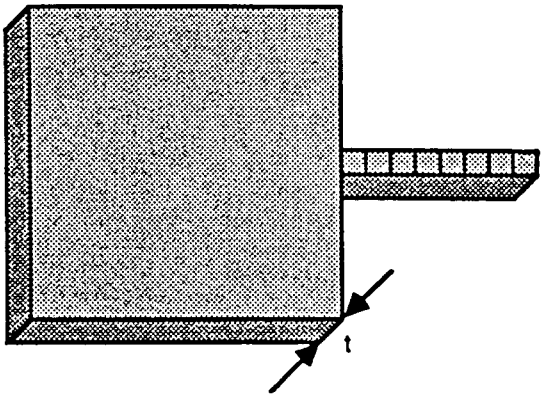

Fig. 2.9
SCF Electrode Pattern

Contamination and imperfections in the metal may result in a higher resistance than computed by Eqs. 2.4a and 2.4b. This parameter was also determined experimentally from the swept S parameters taken away from the filter's passband. Out of the passband the filter behaves as a capacitor to ground with a small series resistance term. One can compute Z_{in} for the filter out of band from Eq. 2.5, and will see that it consists of a small real impedance in series with a negative reactance. The reactive part is due to C_o and the real part is the resistance of R_{met}.

$$Z_{in} = Z_o \times \frac{(1 + S_{11})}{(1 - S_{11})} = R + jX \qquad (2.5)$$

Typical values for R_{met} determined from this measurement technique range from approximately 2.0Ω to 4.5Ω. The inclusion of the parameter R_{met} should be done with caution as the measured value is highly dependent upon the location and contact pressure of the probe tips or the placement of the wire bond on the "pan handle" of the electrode since the greatest number of squares exists there.

2.4. Touchstone Filter Optimization

The capability of Touchstone to model both transmission line effects and lumped elements makes it well suited for microwave filter analysis. In particular, the response of the stacked crystal filter can be studied using Touchstone and in addition, the optimizing routine may be employed to obtain the best set of parameters to model a specific filter and its associated parasitics.

In Eqs. 2.1 through 2.3 which govern the values of the parameters in the equivalent circuit, the values of K and Q are of significant importance. Unfortunately, these values are difficult to measure directly when the resonators are coupled to make a stacked crystal filter, and the stiffness coefficient K may also differ between film layers. Touchstone allows K and Q to range within reasonable limits so that the computed values of R_S, C_S, C_O, and L_S provide the best fit possible to the measured parameters.

Fig. 2.10a is a sample Touchstone input file for a series stacked crystal filter with its nodes numbered in Fig. 2.10b. The first few lines are indicated as comment lines by the ! character and are used to identify the file. Below them is a dimension DIM block which defines the default values for units. Next, the equation EQN block is employed along with the variable VAR block in order to preserve the interdependencies of the element values as given in Eqs. 2.1 through 2.3. The elements of the circuit are listed by their nodes in the circuit CKT block in a similar fashion to that used in SPICE. Parameters may be given constant values or allowed to vary within a specified range in which case three values are needed to define the lower limit, initial value, and upper limit. The output OUT block specifies which parameters will be displayed in a variety of formats including rectangular and Smith Chart displays. The frequency FREQ block determines the sweep range of the analysis and is analogous to setting the frequency range on a network analyzer.

```
Touchstone (TM) -Ver(1.40-Lot 103)-Targ(IBM-PC/AT)-Ser(16678-2619- 1000)
            VCOFILT.CKT    01/04/88 - 10:23:21

! name : VCOFILT
! date : 10-20-88
! purpose: OPTIMIZE MODEL TO S PARAMETER DATA FOR SCF
DIM
  FREQ GHZ
  RES OH
  IND NH
  CAP PF
  LNG MIL
  TIME PS

  ANG DEG
VAR
  C0   # 2.50 3.50   4.50
  K    # .004  0.02     .05
  M    # .900 1.00  1.300
  RS   # 2.00  5.0  20.00
EQN
  C02=C0*2
  CS=k*C0
  LS=M/(.042618*CS)
CKT
  CAP    11 0  C# .03 .05 .07
  IND    11 1  L# 1.0  2.0  4.0
  RES     1  2  R# 1.0  3.00 3.50
  CAP     2 10 C^C0
  CAP     8 10 C^C0
  CAP     5 10 C^C02
  IND    10 0  L# .01 .10  .50
  IND     3  4  L^LS
  RES     2  3  R^RS
  CAP     4  5  C^CS
  IND     6  7  L^LS
  RES     5  6  R^RS
  CAP     7  8  C^CS
  RES     8  9  R#  1.00 3.00 3.50
  IND     9  12  L# 1.0  2.0 4.0
  CAP    12  0  C# .03  .05 .07
  DEF2P  11 12 SCF
  S2PA   20 30  0 VCOFILT
  DEF2P  20 30 REALSCF
```

Fig. 2.10a
Touchstone Circuit File

```
OUT
  SCF DB[S21]  GR2
  REALSCF DB[S21]  GR2
  SCF DB[S22]  GR2
  REALSCF DB[S22]GR2
  SCF  ANG[S21] GR3
  REALSCF ANG[S21] GR3
! SCF  ANG[S22] GR3
! REALSCF ANG[S22] GR3
FREQ
  SWEEP  1.00 1.073 .001
! SWEEP  0.900 1.200 .005
GRID
  RANGE  1.000 1.073 .010


Touchstone (TM) -Ver(1.40-Lot 103)-Targ(IBM-PC/AT)-Ser(16678-2619- 1000)
            VCOFILT.CKT   01/04/88 - 10:23:26

! RANGE  0.900 1.200 .050
  GR1    00  01  .05
  GR2   -30  00  5
  GR3    180 -180 20
OPT
  range 1.020  1.055
  SCF MODEL  REALSCF
```

Fig. 2.10a (continued)

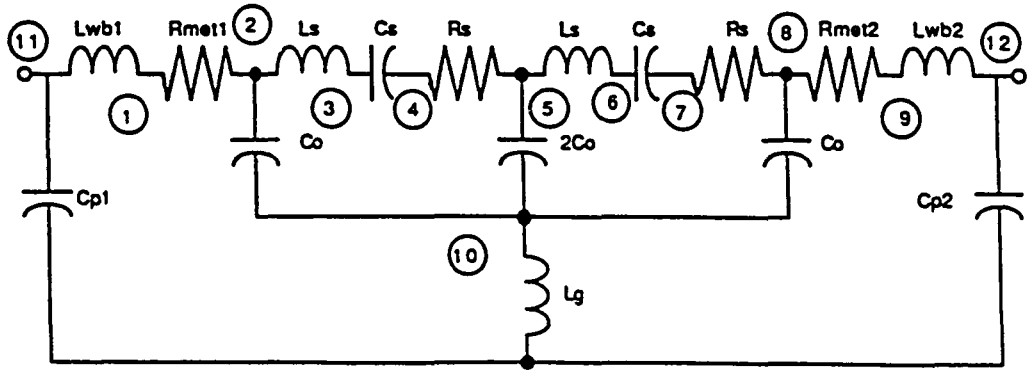

Fig. 2.10 b
Node Numbered Circuit

The grid GRID block enables the user to tailor the display grids, and lastly, the optimize OPT block, instructs the program to perform the optimizing routine according to the statements contained within the block. The frequency range of the optimizer need not be that as specified in the FREQ block as long as it is within that range and may differ in order to weight or emphasize the parameters in a smaller bandwidth such as the passband of the filter. The model statement is included to instruct the optimizing routine to fit the model to the measured values listed in the designated file.

The optimizing routine is initiated by striking the appropriate soft key, and the operator may choose from a random or gradient optimization. The former varies parameters within their designated range at random for a number of specified iterations and stores the combination which resulted in the lowest error term. The latter involves making small perturbations to the initial parameter values, computing an error term, and increasing the perturbation in the same direction if the error term decreases, or reversing the direction of the perturbation if the error term increases. When the optimization is complete, the new file should be swept in frequency to display the model's response. If the response is satisfactory, then the circuit model parameters may be extracted from the file.

In the case where a filter's measured response displays amplitude and phase irregularities such as those caused by filter modes other than the fundamental, it may be beneficial to smooth the measured data in the vicinity of the uncharacteristic response to provide the best overall

fit. It may also be desirable to fix the values of the parasitic elements while optimizing the embedded circuit parameters within a narrow bandwidth around the center frequency, and then to open up the bandwidth of the optimizer to allow the parasitic values to vary while the embedded circuit parameters remain fixed.

Fig. 2.10c is the resulting circuit file after an optimization run was completed on the filter used in the VCO design as discussed in Chapters 4 and 5. The middle values of the variable elements are those which resulted in the best fit and may be extracted for use in further analysis. Figs. 2.10d and e show the resulting magnitude and phase plots for S_{21} and S_{22} as computed from the model along with the actual measured values, respectively. Fig. 2.10f is a wideband magnitude plot which shows the effect of modeling the package parasitics. It is seen that the filter is well modeled within the passband, and the phase of S_{21} which is an important parameter in determining the filter's Q and, consequently, the stability of the oscillator is nearly identical to the measured response. Outside the passband, the parasitic elements account for the filter's behavior. This example is typical of the degree of accuracy which may be obtained in optimizing the equivalent circuit of a filter to its measured parameters. It is also seen to be useful in the characterization of parasitic effects and in determining the effective Q and K for the filter which may be extracted using Eqs. 2.1 through 2.3 once the element values are known.

```
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! name : VCOFILT
! date : 10-20-88
! purpose: OPTIMIZE MODEL TO S PARAMETER DATA FOR SCF
DIM
  FREQ GHZ
  RES OH
  IND NH
  CAP PF
  LNG MIL
  TIME PS

  ANG DEG
VAR
! C0   # 2.50 3.84476   4.50
! K    # .004  0.02056     .05
! M    # .900 1.03189  1.300
! RS   # 2.00  10.42194  20.00
  C0 = 3.84476
  K = .02056
  M = 1.03189
  RS = 10.42194
EQN
  C02=C0*2
  CS=k*C0
  LS=M/(.042618*CS)
CKT
  CAP    11 0  C# .03 0.05076 .07
  IND    11 1  L# 1.0  1.71227  4.0
  RES    1  2  R# 1.0  2.70984 3.50
  CAP    2 10 C^C0
  CAP    8 10 C^C0
  CAP    5 10 C^C02
  IND    10 0  L# .01 0.09777  .50
  IND    3  4  L^LS
  RES    2  3  R^RS
  CAP    4  5  C^CS
  IND    6  7  L^LS
  RES    5  6  R^RS
  CAP    7  8  C^CS
  RES    8  9  R#  1.00 2.80994 3.50
  IND    9  12  L# 1.0  2.08547 4.0
  CAP    12  0  C# .03  0.05099 .07
  DEF2P  11 12 SCF
  S2PA   20 30  0 VCOFILT
  DEF2P  20 30 REALSCF
```

Fig. 2.10c
Optimized Circuit File

```
OUT
  SCF DB[S21]  GR2
  REALSCF DB[S21]  GR2
  SCF DB[S22]  GR2
  REALSCF DB[S22] GR2
  SCF  ANG[S21] GR3
  REALSCF ANG[S21] GR3
! SCF  ANG[S22] GR3
! REALSCF ANG[S22] GR3
FREQ


Touchstone (TM) -Ver(1.40-Lot 103)-Targ(IBM-PC/AT)-Ser(16678-2619- 1000)
            VCOPT.CKT    01/04/88 - 10:32:15

! SWEEP  1.00 1.073 .001
  SWEEP  0.900 1.200 .005
GRID
! RANGE  1.000 1.073 .010
  RANGE  0.900 1.200 .050
  GR1     00  01  .05
  GR2    -50  00  5
  GR3     180 -180 20
OPT

  SCF MODEL  REALSCF
```

Fig. 2.10c (continued)

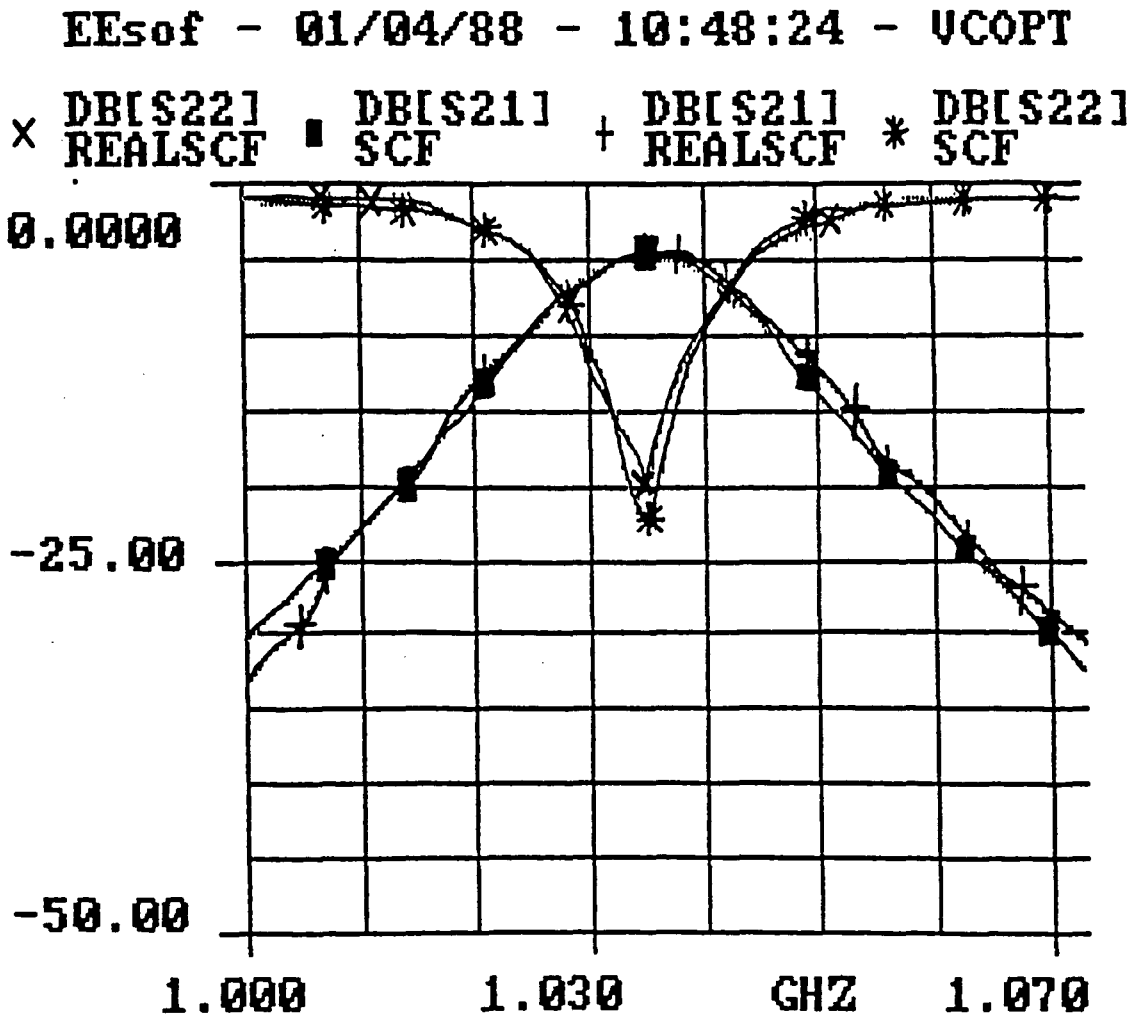


Fig. 2.10d
Magnitude Plot of Measured (REALSCF) and Computed (SCF) S_{21} and S_{22}

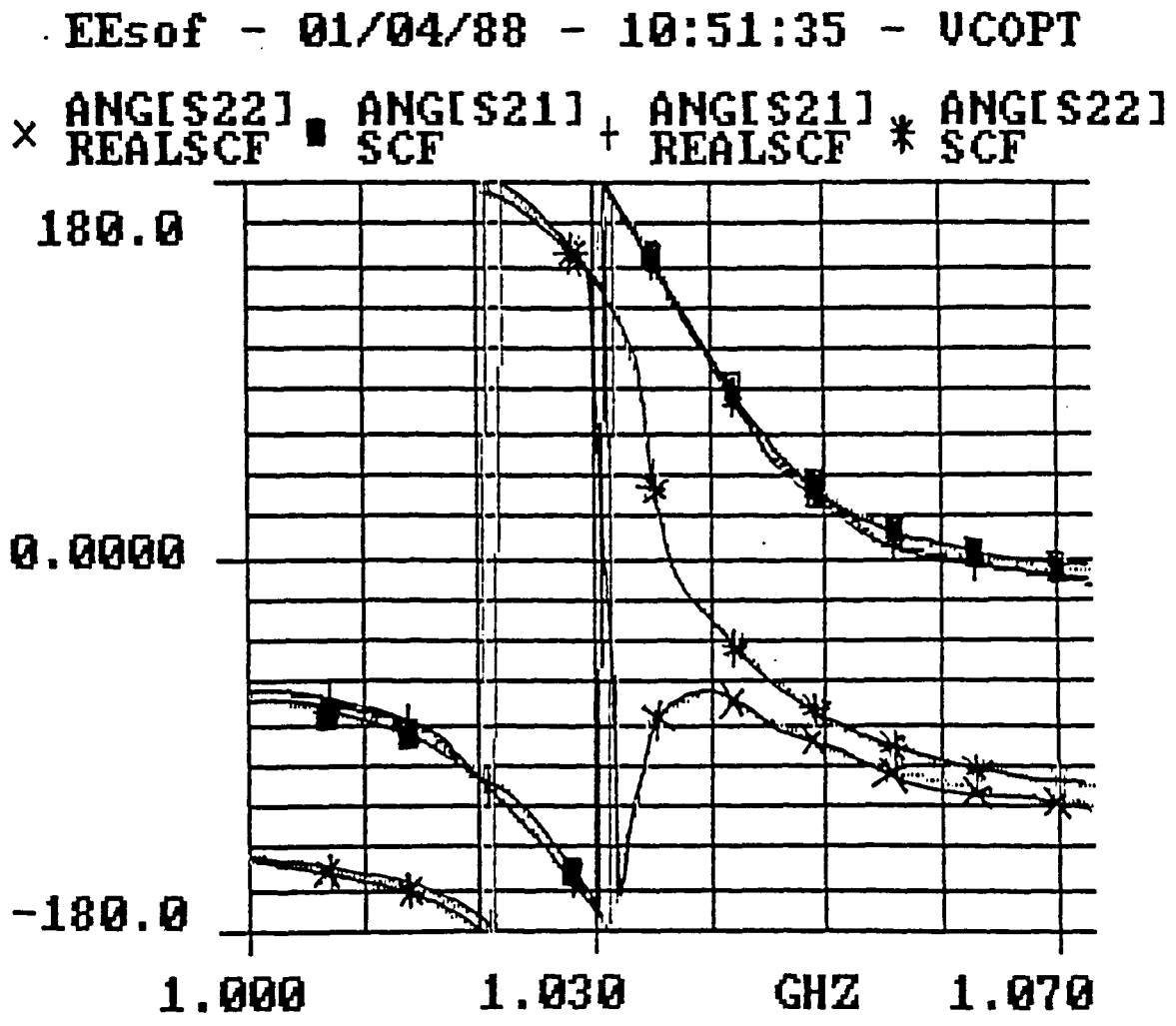


Fig. 2.10e
Phase Plot of Measured (REALSCF) and Computed (SCF) S_{21} and S_{22}

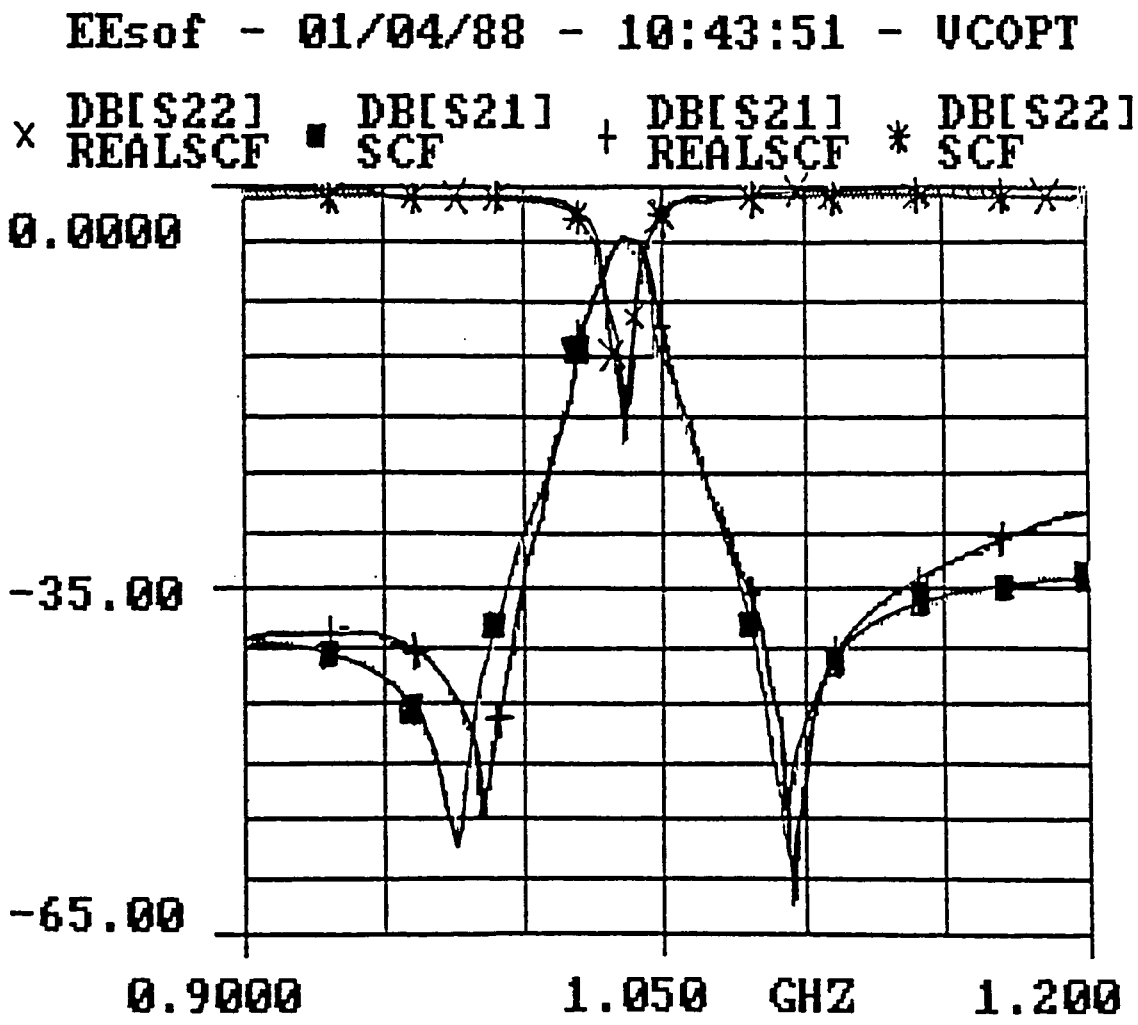


Fig. 2.10 f
Wideband Magnitude Plot

3. OSCILLATOR DESIGN METHODS

3.1. Simple Oscillator Design

Fig. 3.1 is a block diagram representation of a feedback circuit which may be used to model a simple oscillator circuit. Using basic linear feedback analysis, one can analyze the stability of such a circuit to determine whether or not it will sustain oscillation at a certain frequency f_o. To simplify the analysis we assume that the amplifier block, G, has gain only in the forward direction, and further, that there are no reflections due to impedance mismatches. With these assumptions in mind, the conditions necessary to sustain oscillation are those which satisfy the Barkhausen criteria given in Eqs. 3.1 and 3.2.

$$|G|\ |H| = 1 \tag{3.1}$$

$$\phi_G + \phi_H = 0 \tag{3.2}$$

Simply stated, the gain of the amplifier must be great enough to overcome the losses in the feedback element, H, and the sum of the phase contributions must be 0 or multiples of 2π radians. The above assumptions may seem restrictive, and indeed they are in general at microwave frequencies, but in the special case where an impedance matched amplifier and feedback network are employed, the above equations can be used to closely predict the frequency of oscillation for a simple oscillator circuit, although a more complete analysis will be presented in Section 3.2.

A convenient feature of the stacked crystal filters is that they may be designed to have an input impedance of 50Ω in the center of the passband. This is evidenced by a polar display of S_{11} for a typical series stacked crystal filter shown in Fig. 3.2. The same can be said for the output impedance due to the high degree of symmetry of the filter. Microwave amplifiers are typically designed to be impedance matched to 50Ω as well and are readily available by a number of manufacturers. A popular series of amplifiers, MAR 1 through MAR 8, manufactured by Mini Circuits, were used in the design of the circuits reported on in this thesis. Characteristic of this series are bandwidths of up to 2 GHz., S_{11}, S_{22}, and S_{12} below -15 dB, and S_{21} or forward transmission of 10 dB or greater. The reader is referred to Appendix A for details on microstrip design, amplifier biasing and amplifier specifications.

The amplifiers used approach the ideal amplifier indicated in Fig. 3.1 and may be characterized by letting $|G|$ equal $|S_{21}|$ and ϕ_G equal ϕ_{S21}. The feedback block, H, consists of the stacked crystal filter and a section of transmission line of appropriate length so that $|H|$ equals the insertion loss of the filter and ϕ_H equals the phase of the filter at the center of its passband plus the added phase of the transmission line.

Insertion loss in the stacked crystal filters is typically in the range of 3 to 6 dB with the best devices achieving values as low as 1.9 dB [9]. Additional losses, approximately 3.5 dB, result from the power splitting necessary to provide an output signal from the oscillator.

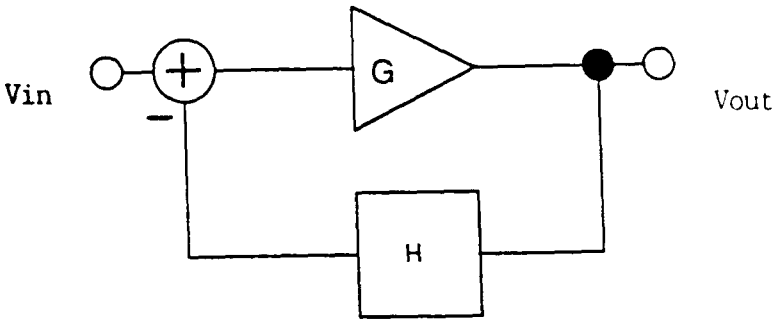


Fig. 3.1
Simple Feedback Circuit

fc = 1035 MHz
± 100 MHz

Fig. 3.2
Polar Display S_{11}

Since the open loop gain in the amplifier will always be slightly greater than the losses in the feedback network, a saturation condition must exist in the amplifier. This fact violates the assumption of linear analysis and complicates the design procedure, although the presence of the excess gain becomes a useful artifact in the operation of a voltage controlled oscillator as discussed later.

In a departure from linear circuit analysis, the effect of the saturating amplifier may be accounted for in the simple oscillator circuit. The excess gain of the amplifier causes it to be driven into compression, the maximum output level attainable for a given bias condition, and it is this nonlinearity that contributes to harmonic generation and spectral broadening [12]. It is a good approximation to treat the other circuit elements as linear devices. A study of the performance of TFR based filters under elevated power levels indicated that the characteristics of the stacked crystal filter changed only slightly at input power levels greater than 25 dBm [13]. The oscillator circuits studied are designed to deliver power of less than 10 dBm which is well within the linear range of the filters. The S parameters of the amplifier, especially S_{21} may differ dramatically from those measured at low incident power. The full S matrix cannot be determined by direct measurement on a network analyzer for an amplifier since power must be incident at port 2 for measurement of S_{22} and S_{12} which removes the driving signal from port 1, making the over-driving of the amplifier impossible. A technique for acquiring the full S matrix is presented in Appendix C and the design procedure has been extended to include the

large signal effect of the full S matrix. For the purposes of the simple oscillator circuit, however, the characterization of S_{21} as the amplifier is driven into compression is sufficient and provides a useful means of predicting the output power of the oscillator. The measurement set up shown in Fig. 3.3 was used to study the variation of S_{21} for increasing levels of input power. Incident power on the DUT was determined by adding the gain in dB of the external amplifier to the output power of the HP8505A RF source and subtracting the losses due to attenuation and power splitting inside the HP8503 S parameter test set. The operator is cautioned to keep power levels below the maximum input ratings and to pad the inputs to the network analyzer. In addition, the measurements should be treated as time averages of the amplitude and phase deviations present which contribute to the frequency fluctuations of the oscillator.

In order to provide a small amount of tunability to the oscillator circuit, a capacitor was later included in series with the feedback network. Tuning the oscillator allows for the compensation of environmental effects on the oscillator such as temperature, humidity, loading, and bias changes. To understand the effect of adding series capacitance, consider the two port representation of Fig. 3.4, of a series capacitor. We can derive the two port parameters to obtain the expressions in Eqs. 3.3 through 3.5 with $Z_{o1} = Z_{o2} = 50\Omega$.

$$\text{ARG}\{S_{21}\} = \text{ARG}\{S_{12}\} = \tan^{-1}(X_c/100) \tag{3.3}$$

$$|S_{21}| = |S_{12}| = 100/(100^2 + X_c^2)^{1/2} \tag{3.4}$$

$$|X_c| = 1/(2\pi \times f \times C) \qquad (3.5)$$

The effect on the circuit may differ since the input and output impedance of the filter and amplifier are not ideally 50Ω, but Eq. 3.3 give a good approximation of the amount of phase shift one can accomplish with a variable series capacitance. Fig. 3.5 illustrates the effect of a series capacitance on the filters characteristic as observed in an open loop configuration. Notice that the filter's Q, phase slope, and insertion loss increase with decreasing C. A capacitance that could be varied from 4 to 18 pF would allow a change in open loop phase of 26° which would result in a frequency of oscillation change of approximately 3 MHz considering a typical phase slope for a SCF of 9 °/MHz, and provided that the phase slope of the filter remains the same in a closed loop configuration.

The method of adjusting the frequency of an oscillator with a series capacitance is referred to as "pulling" and is a common practice used in industry to accomplish small frequency shifts [14, p. 122]. Of course the tuning range of an oscillator depends on the phase slope of the filter or resonator, and since the phase slope of the composite devices such as the stacked crystal filter are fairly low, we can achieve a usable amount of frequency change on the order of .5% for a series SCF and 1% for a single SCF.

3.2. VCO Design

Instead of manually adjusting a variable capacitor to accomplish frequency tuning, it would be preferable to use a device that displays a

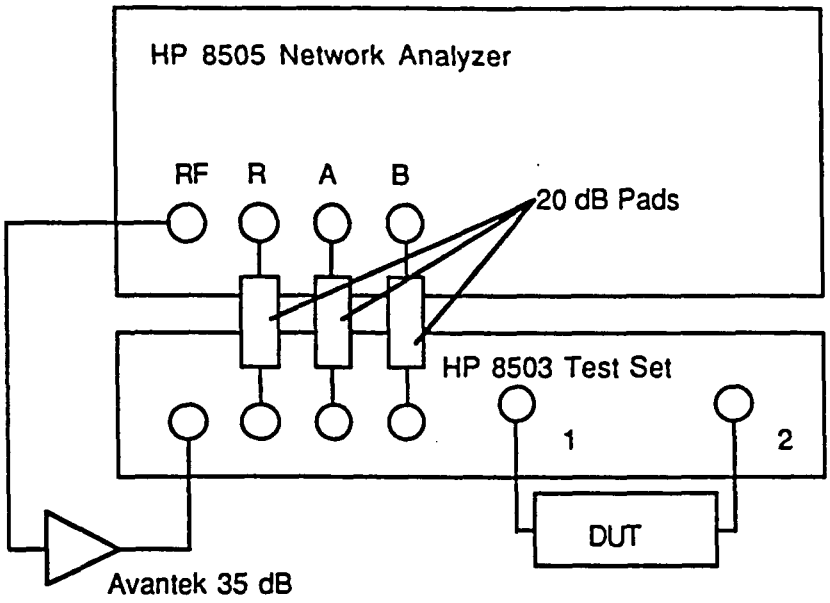


Fig. 3.3
Large Signal Measurement Setup

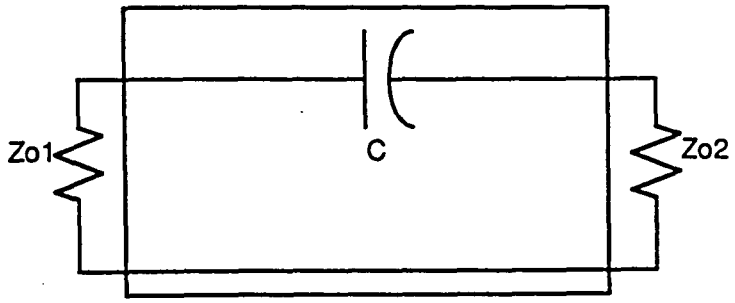
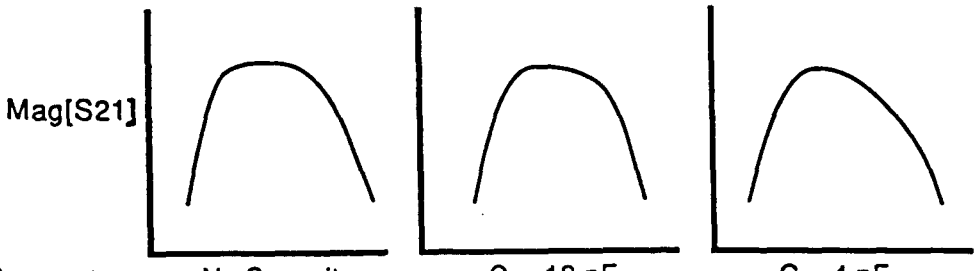


Fig. 3.4
Series Capacitor



Parameter	No Capacitor	C = 18 pF	C = 4 pF
Q	65.3	66.5	72.3
Phase slope deg/MHz	8.08	8.11	8.21
Insertion Loss dB	6.2	6.7	8.0

Fig. 3.5
Effect of Series C

voltage variable reactance. Capacitances on the order of one to tens of pF are typical of the junction capacitances of discrete semiconductor diodes.

In particular, a family of diodes are designed to exploit the capacitance vs. voltage dependence of the semiconductor junction. The term varactor comes from the words variable and reactance and refers to a device whose reactance can be varied in a controlled manner with a bias voltage [15, p. 114]. The C - V law of a diode may be understood by considering the effect of bias voltage on the depletion layer width of a semiconductor junction. If we represent the depletion region of a diode as a parallel plate capacitor, then assuming that the permittivity and cross sectional area of the depletion area remain constant with voltage, the voltage dependence of the junction capacitance can be related to the voltage dependence of the depletion layer thickness $D(V_j)$ according to Eq. 3.6 where $V_j = \Psi_o - V_a$, Ψ_o is the built in potential, and V_a is the applied voltage (positive for forward bias).

$$C(V_j) = \varepsilon A/D(V_j) \tag{3.6}$$

The depletion layer thickness also depends on the doping profile used in the device fabrication. Eqs. 3.7 through 3.9 give the $D(V_j)$ relation for three different doping profiles [16, p. 30].

$$\text{ABRUPT} \qquad D(V_j) \propto (V_j)^{1/2} \tag{3.7}$$

$$\text{LINEAR GRADED} \qquad D(V_j) \propto (V_j)^{1/3} \tag{3.8}$$

$$\text{HYPERABRUPT} \qquad D(V_j) \propto (V_j)^{x} \qquad 1/2 < x < \infty \tag{3.9}$$

The exponent, x is a function of voltage for the hyperabrupt junction diode and may behave as shown in Fig. 3.6. Substituting $D(V_j)$ into Eq. 3.6 leads to the C - V relation for the following three cases in Eqs. 3.10 through 3.12 [15, p. 115].

$$\text{ABRUPT} \qquad C(V_j) \propto (V_j)^{-1/2} \tag{3.10}$$

$$\text{LINEAR GRADED} \qquad C(V_j) \propto (V_j)^{-1/3} \tag{3.11}$$

$$\text{HYPERABRUPT} \qquad C(V_j) \propto (V_j)^{-x} \tag{3.12}$$

Fig. 3.7 illustrates the C - V curves for the three cases as mentioned. It is obvious that the hyperabrupt junction diode allows for the greatest variation in capacitance for a given voltage change. DKV4105 and 4109 series varactor diodes manufactured by Alpha Semiconductor were chosen to be used as the tuning element in the VCO. The C - V relationship was measured using an HP4280A C - V Plotter at 1 MHz where the the capacitance ranged from tens of pF at 0 V bias to a few pF at 20 V reverse bias. In addition to this, a test fixture was built to measure the S parameters of the diodes at various bias voltages in the vicinity of the oscillator's operating frequency. Fig 3.8 shows a polar display of S_{21} for the varactor network at various bias voltages. Varying the reverse bias from 0 to 20 volts allows for a net phase change of approximately 32° which should allow approximately 3.5 MHz of tuning when used in series with a series stacked crystal filter with a phase slope of approximately 9°/MHz.

The unloaded Q of the stacked crystal filter may be determined from the phase slope by Eq. 3.13 where ϕ is in radians.

$$Q_{UL} = (f_o \times \Delta\phi)/2\Delta f \tag{3.13}$$

When used as the feedback element in an oscillator, the loaded Q of the filter must be determined for the purposes of noise and frequency stability analysis. The loaded Q, Q_L, will be less than that of the unloaded filter and will also be a determining factor in predicting the tunability of the oscillator since a lower value of Q corresponds to a lower phase slope, hence an increased tuning range.

In designing the simple oscillator circuits, the assumptions of negligible reverse transmission and reflections at impedance mismatches were made and were seen to be reasonable. In the case of designing a voltage controlled oscillator using a varactor tuning diode, a more general approach was used. Fig. 3.9 is a block diagram of a closed loop oscillator which is driving a 50 Ω load which may represent the input to a spectrum analyzer, counter, or buffer amplifier. Provided that the closed loop operating conditions of the individual elements in the circuit could be preserved upon opening the loop at any point, as shown in Fig. 3.10, a necessary condition for oscillation would be that of Eq. 3.14a and likewise, that of Eq. 3.14b.

$$a_1 = b_2 \tag{3.14a}$$

$$a_2 = b_1 \tag{3.14b}$$

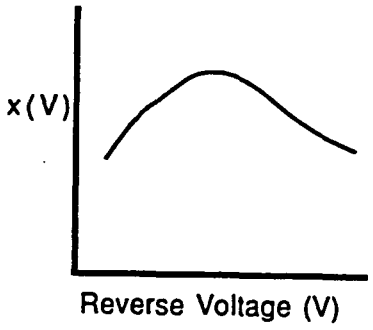


Fig. 3.6
Variation of Exponent

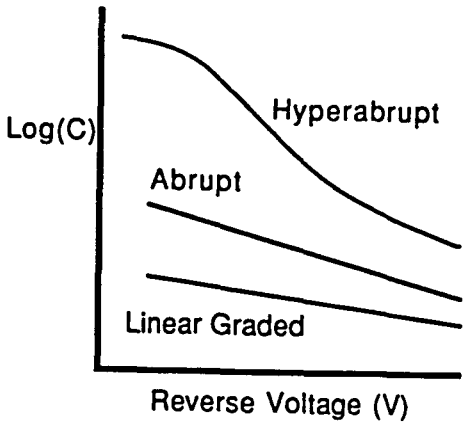


Fig. 3.7
C - V Law

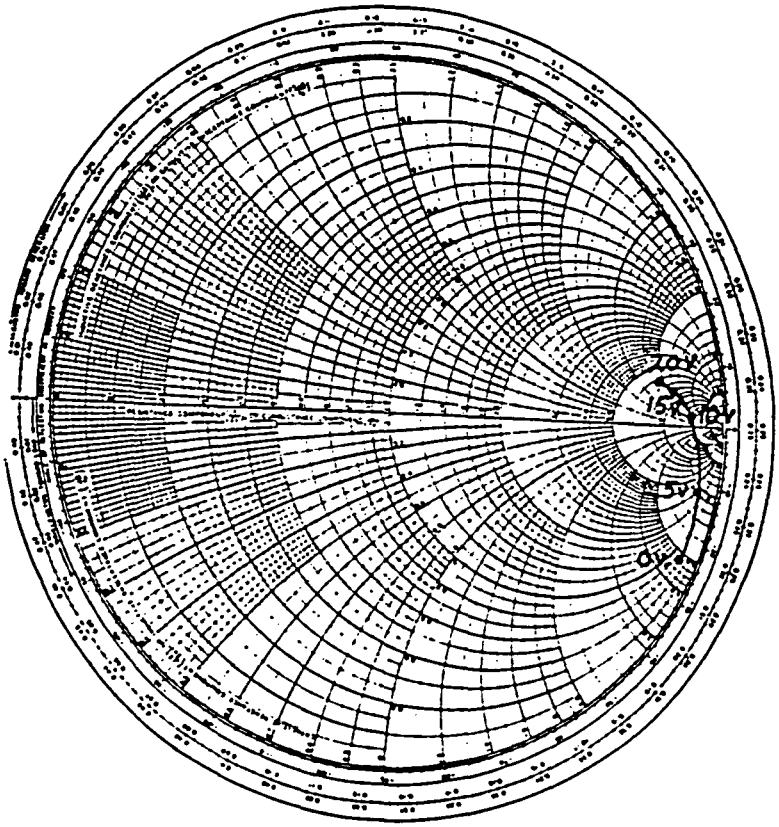


Fig. 3.8
Polar Display of Varactor S_{21}

If the individual S parameters of the amplifier, SCF, varactor, etc., are known, the net two port S parameters for the open loop oscillator may be determined, and the following expressions may be derived:

$$b_2 = a_1 = S_{21}a_1 + S_{22}a_2 \tag{3.15a}$$

$$b_1 = a_2 = S_{11}a_1 + S_{12}a_2. \tag{3.15b}$$

Solving Eqs. 3.15a and 3.15b for a_1 respectively yields:

$$a_1 = S_{22}a_2/(1 - S_{21}) \tag{3.16a}$$

$$a_1 = a_2(1 - S_{12})/S_{11}. \tag{3.16b}$$

Equating the two expressions gives the general condition for oscillation of Eq. 3.17.

$$S_{22}S_{11} = 1 - S_{12} - S_{21} + S_{12}S_{21} \quad \text{or} \quad 1 = \Delta S + S_{12} + S_{21} \tag{3.17}$$

Where $\Delta S = S_{11}S_{22} - S_{12}S_{21}$ [17]. It should be noted that for the case where S_{11}, S_{22}, and S_{12} are zero, the above condition reduces to the Barkhausen criteria of Eqs. 3.1 and 3.2. For the case of the simple oscillator, the only large signal parameter measured for the amplifier was S_{21}. The above analysis requires that a full S parameter matrix be measured or calculated for each circuit element so that the net two port open loop S parameters may be computed. In the case of the amplifier, a perturbational method for obtaining large signal S parameters may be used and is described in Appendix C. As before, all other circuit elements are considered to be linear and the S parameters may be calculated or measured directly. The individual S parameters should be

taken within the passband of the filter used and the overall S parameter matrix may be computed. Touchstone may be used to greatly simplify this chore, and in addition the electrical length of the transmission line in the feedback path may be tuned to satisfy Eq. 3.2 at the desired frequency. The degree of compression that the amplifier is operating at may be estimated, and the appropriate large signal parameters describing this condition may be used. This may be an iterative process. Finally, the condition of Eq. 3.17 for the overall open loop circuit will verify that oscillation at the predicted frequency will indeed occur.

3.3. Use of the Overmoded Filter in Oscillator Designs

Fig. 3.11 is a block diagram used to design a highly stable fundamental mode oscillator using the overmoded stacked crystal filter as the feedback element. The overmoded filter provides the designer with a bandpass filter bank with center frequencies at approximately 4 MHz intervals as shown in Fig. 3.12. Within a range of 10 to 20 MHz, the characteristics of the individual modes are virtually the same which leads to the problem encountered in designing overmoded structure based oscillators. In the past, oscillators have been constructed using the overmoded filter structure, but it was not possible to achieve single frequency oscillations [5]. Since the amplitude and phase characteristics are similar for adjacent modes, Eq. 3.1 may be satisfied at a number of modes, and the phase condition is that of Eq. 3.2 as modified in Eq. 3.18 where f_n is the frequency of any one of the modes of the overmoded filter and τ_d is the time delay related to the phase slope of one of the modes.

$$2\pi f_n \tau_d + \phi_H + \phi_G = 2n\pi \qquad (3.18)$$

If a delay filter were used in series with the overmoded filter, then an oscillator could be designed to satisfy the conditions necessary to sustain oscillation at a single mode. The series stacked crystal filter allows for a convenient means of introducing delay within the passband of the filter [17]. The remainder of the oscillator design is essentially the same as the simple oscillator circuit which involves adding an appropriate amount of electrical length in series with the feedback network to achieve 0° of phase.

If the stacked crystal filter's passband envelopes more than one mode of the overmoded filter, it may be possible to tune between adjacent modes. This technique is the basis for designing a frequency hopping oscillator that would exhibit a high degree of stability at a given mode due to the high value of Q inherent in the overmoded structure.

A test fixture allows the overall amplitude and phase response of the overmoded and stacked crystal filter cascaded with a series stacked crystal filter shown in Fig. 3.13 to be determined. The net insertion loss may be determined along with the overall unloaded Q of the two filters in cascade.

3.4. Design Summary

In summary, this chapter has addressed the design of high frequency oscillators using TFR technology for three different cases. First, an extremely simplified analysis was justified and then described for

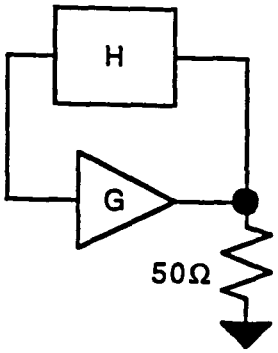


Fig. 3.9
Closed Loop Oscillator

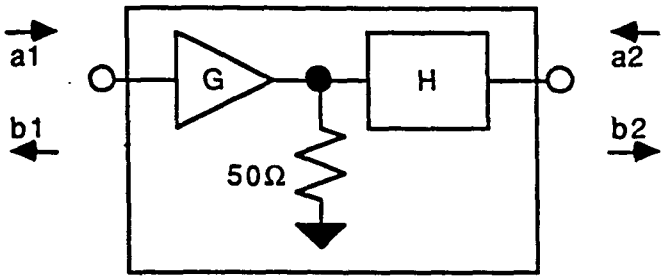


Fig. 3.10
Open Loop Oscillator

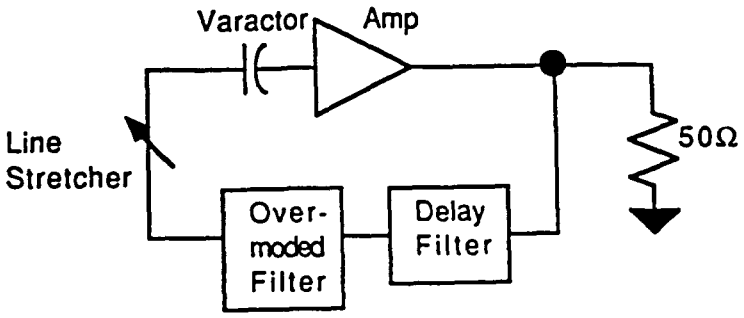


Fig. 3.11
Overmoded SCF Based Oscillator

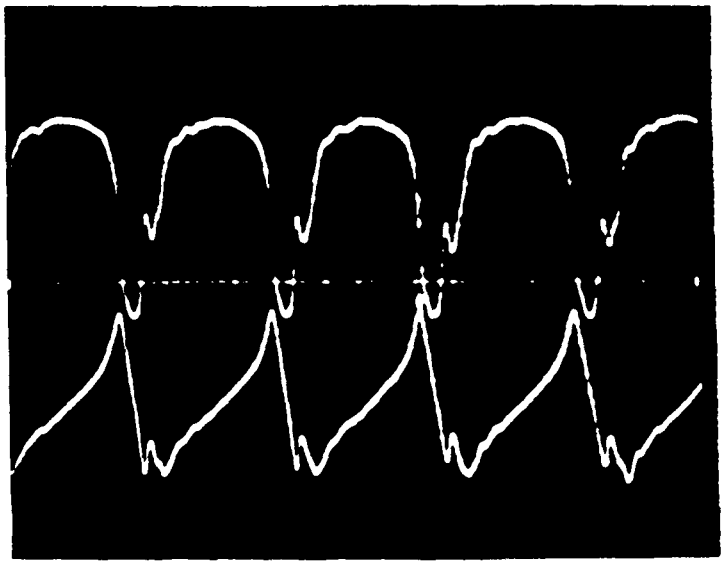


Fig. 3.12
Overmoded SCF Phase (Upper) and Magnitude (Lower)

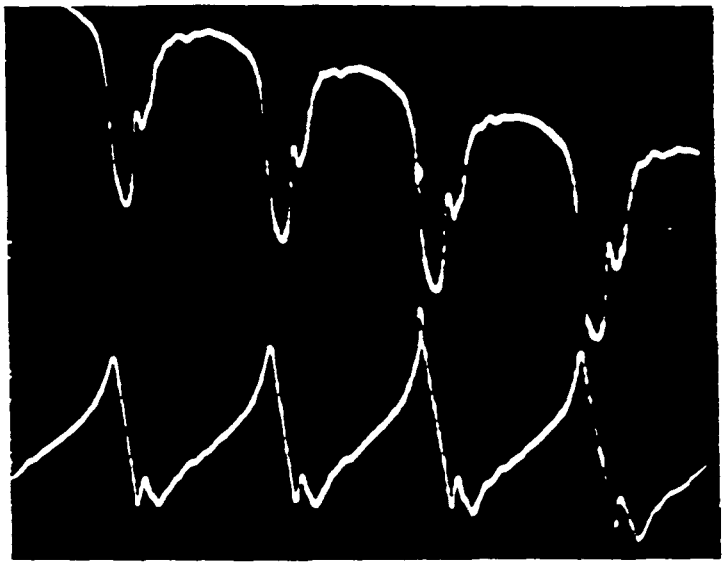


Fig. 3.13
Overmoded SCF in Cascade with SCF Phase (Upper) and Magnitude (Lower)

designing a simple free running oscillator. A provision for tuning was discussed which led to the design of a voltage controlled oscillator. The VCO analysis became more involved and included a perturbational method for obtaining large signal S parameters. Lastly, the design of a low phase noise oscillator using the overmoded filter structure was presented as an extension of the two previous designs. The following two chapters will report on actual examples of these three types of oscillators comparing predicted and measured performance and describing the spectral purity of the oscillators in terms of their respective phase noise.

4. OSCILLATOR DESIGN EXAMPLES

4.1. Simple Oscillator Design Example

Figs. 4.1a and b show the measured amplitude and phase response of the stacked crystal filter used in the construction of the simple oscillator and the response of the lumped equivalent circuit model as optimized on Touchstone using the methods discussed in Chapter 2, respectively. The individual element values for the model are listed in Table 4.1 and were used to model the SCF in a SPICE simulation. A transistor level model of the amplifier was derived and consists of two Darlington connected transistors with resistive feedback. Results of the closed loop simulation are shown in Fig. 4.2 where the phase is seen to cross zero and the loop gain is seen to be great enough to overcome the feedback circuit's losses at 1037 MHz. At this frequency, the Barkhausen criteria discussed in Chapter 3 is satisfied, thus predicting the frequency of oscillation.

The specified maximum output power for this series of amplifiers from the supplied data sheet is 4 dBm. Assuming an ideal power split of power into two 50Ω loads, corresponding to the feedback network and the external load, the power supplied to the external load should be approximately 3.5 dB lower than the output power supplied by the amplifier. Since the amplifier operates at a saturation condition, it was predicted that it would limit at its maximum rating. The power delivered to the external 50Ω load was estimated to be 4dBm - 3.5 dB = 0.5 dBm.

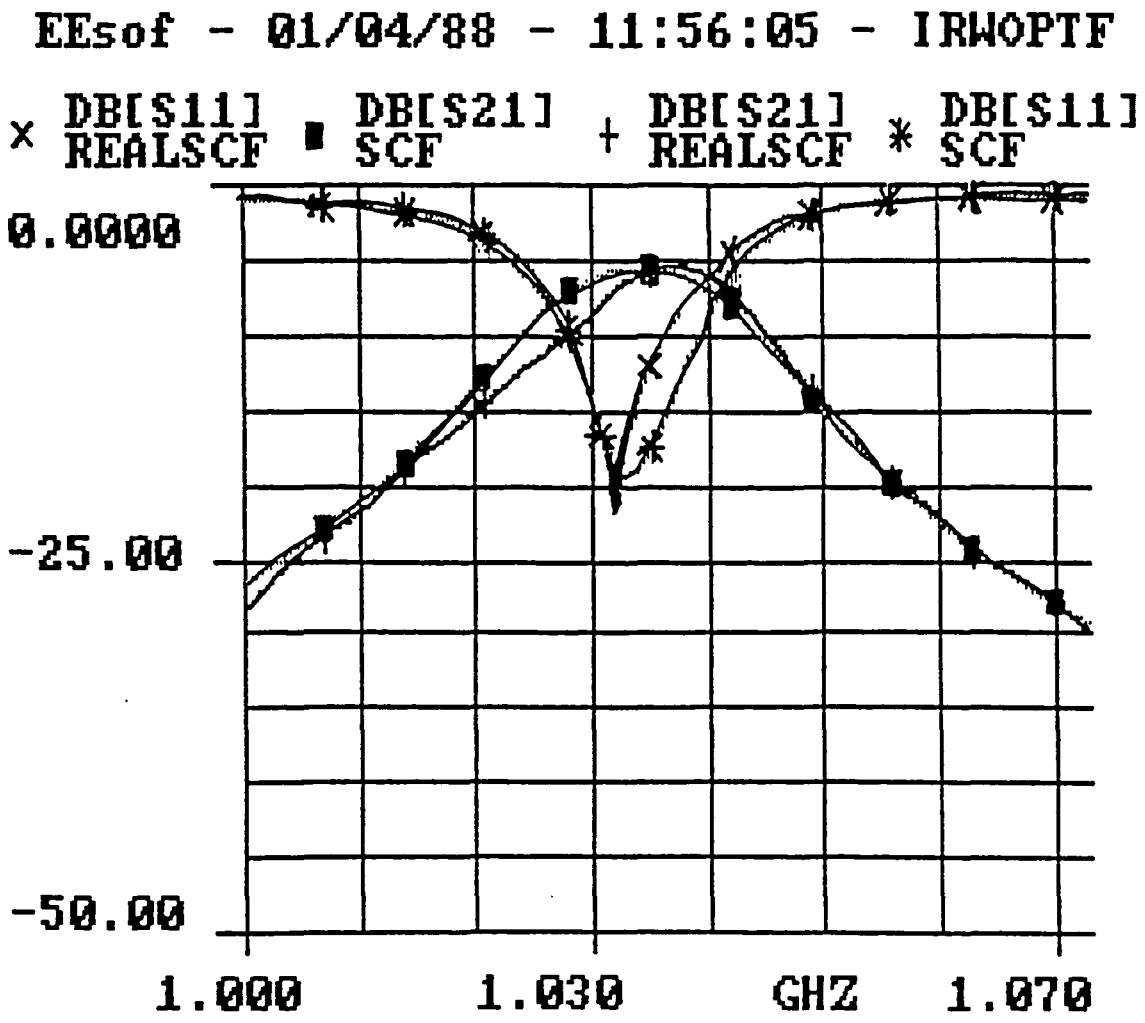


Fig. 4.1a
Magnitude Plot of Measured (REALSCF) and Computed (SCF) S_{21} and S_{11}

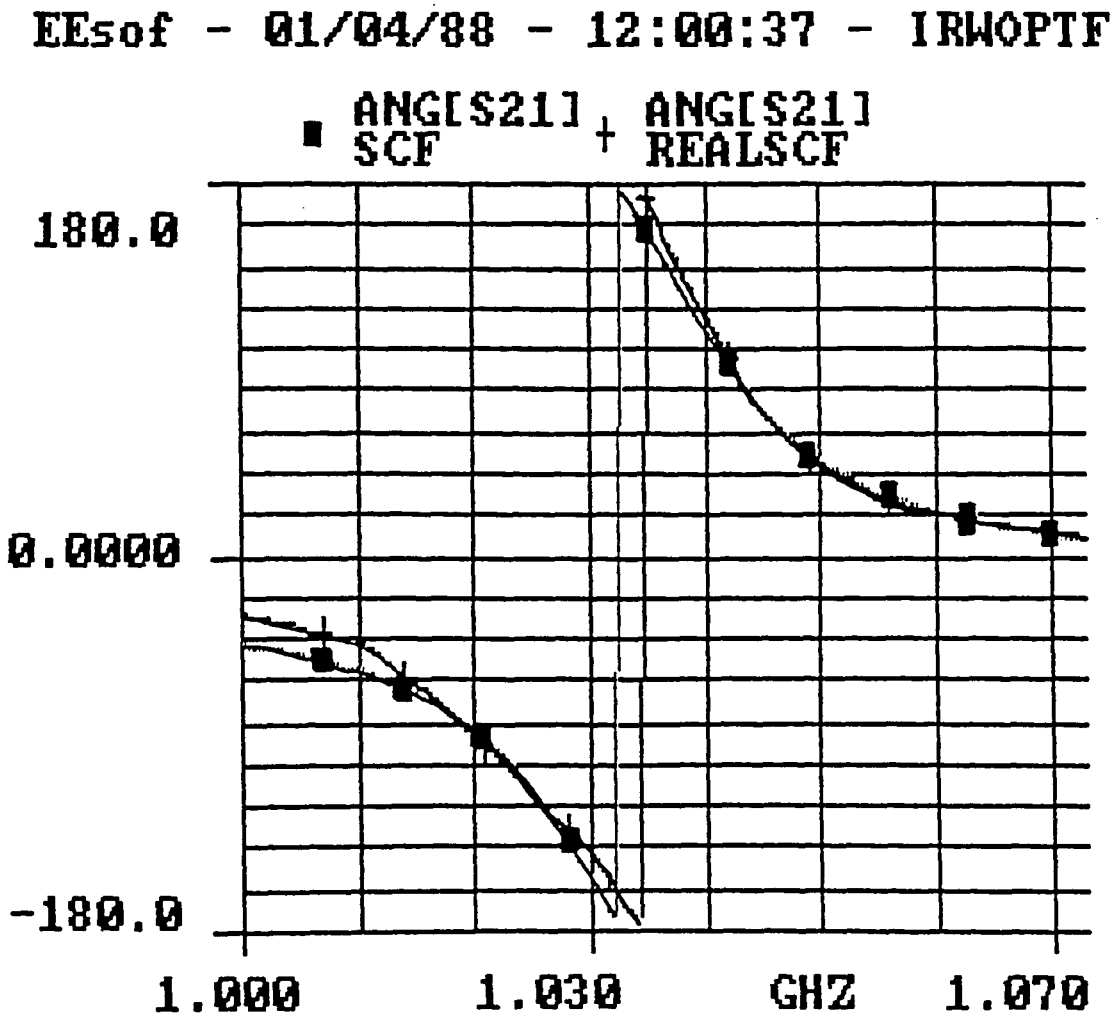


Fig. 4.1b
Phase Plot of Measured (REALSCF) and Computed (SCF) S_{21}

Table 4.1 Lumped Element Model Values

Element Name	Value	Units
R_{met1}	2.6890	Ω
R_{met2}	2.6908	Ω
C_{o1}	3.8376	pF
C_{o2}	3.8287	pF
$2C_o$	7.6663	pF
R_{s1}	12.220	Ω
R_{s2}	12.150	Ω
L_{s1}	290.99	nH
L_{s2}	291.71	nH
C_{s1}	0.08335	pF
C_{s2}	0.08316	pF
C_{p1}, C_{p2}	-	-
L_{wb1}, L_{wb2}	-	-
L_g	-	-

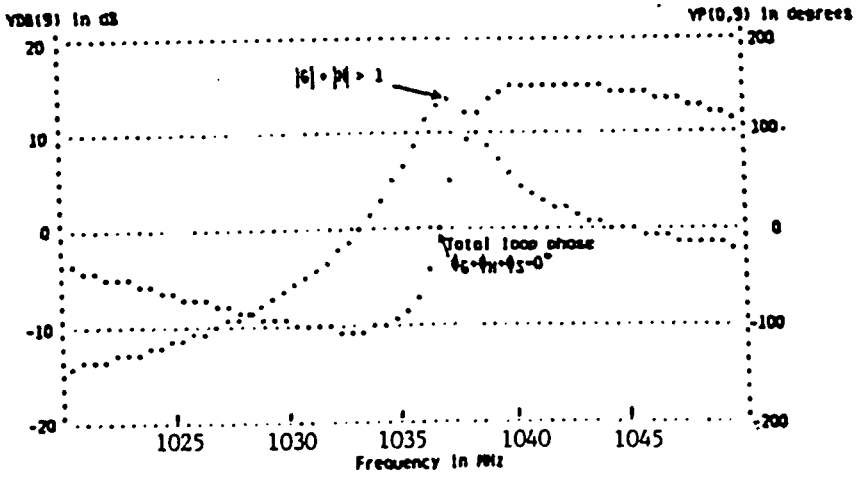


Fig. 4.2
Results from SPICE Analysis

The oscillator's output spectrum was observed on an HP8569 Spectrum Analyzer. A trimming capacitor in series with the feedback network allowed for small frequency adjustments. The oscillator was adjusted for maximum output power which was measured as 5 dBm at 1043.1 MHz. This was above the predicted frequency of 1038 MHz, and in fact it was not possible to tune the oscillator low enough to reach the predicted frequency. Second and third harmonics were measured as -15 dBm and -17 dBm respectively.

The discrepancy between predicted and measured frequency of oscillation is a consequence of the simplifications made in the design and analysis of Chapter 3. In particular, assuming S_{11} and S_{22} to be zero most likely introduced enough error to account for the 5 MHz difference in frequency. Although this error is only .5%, it is great enough to have a serious effect on the oscillator's predicted performance. Output power was also higher than expected and may be explained by differences in maximum output power for individual amplifiers from the specified value given in the data sheet. Harmonic generation was observed to be unacceptably high and may indicate that oscillations are being supported at higher filter modes.

4.2. VCO Design Example

The filter used in the VCO design was presented as an example in Chapter 2 and the results of the optimization along with the measured response are repeated in Figs. 4.3a and b. The element values for the equivalent circuit are listed in Table 4.2. It should be noted that a very good fit to the measured data was obtained, and in particular, the

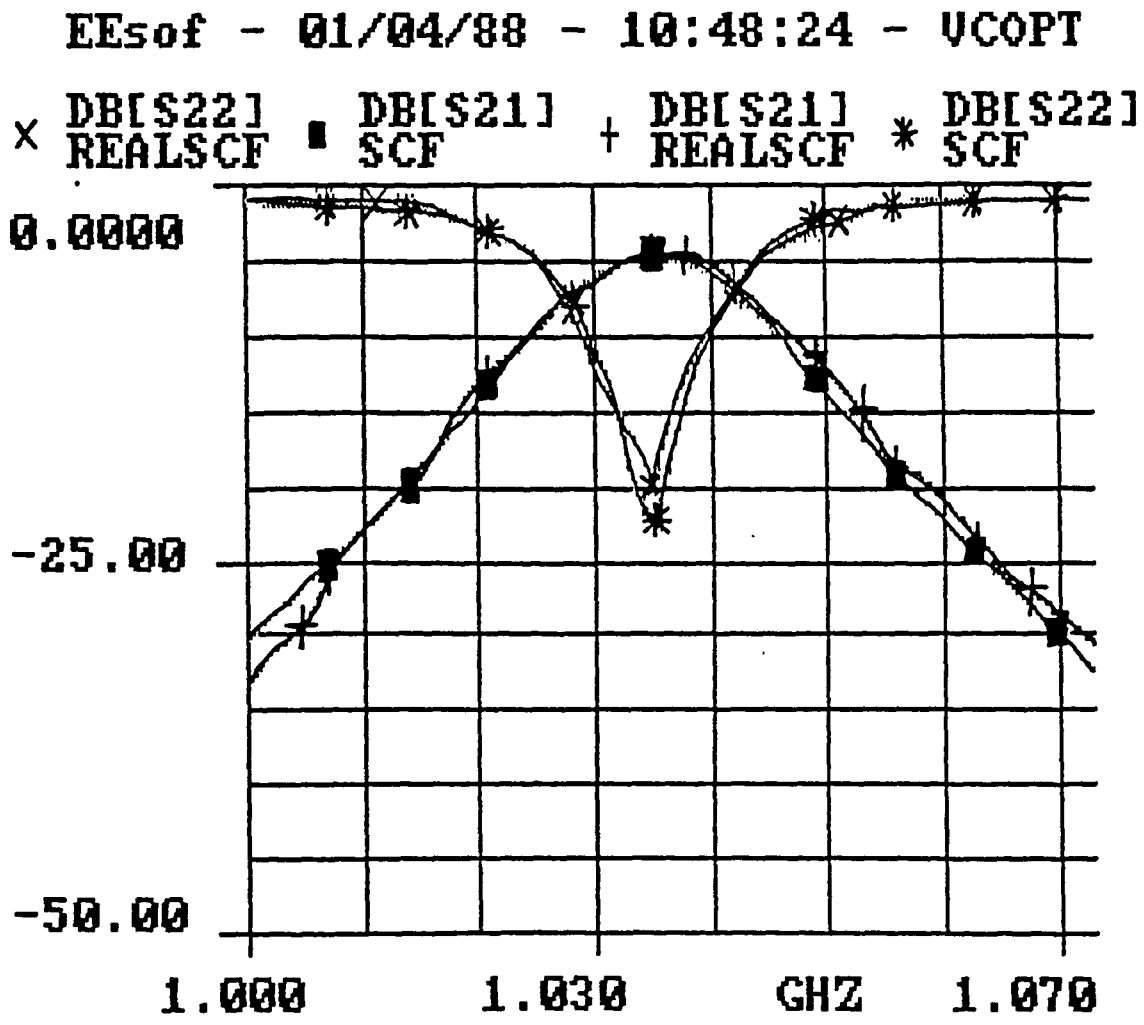


Fig. 4.3a
Magnitude Plot of Measured (REALSCF) and Computed (SCF) S_{21} and S_{22}

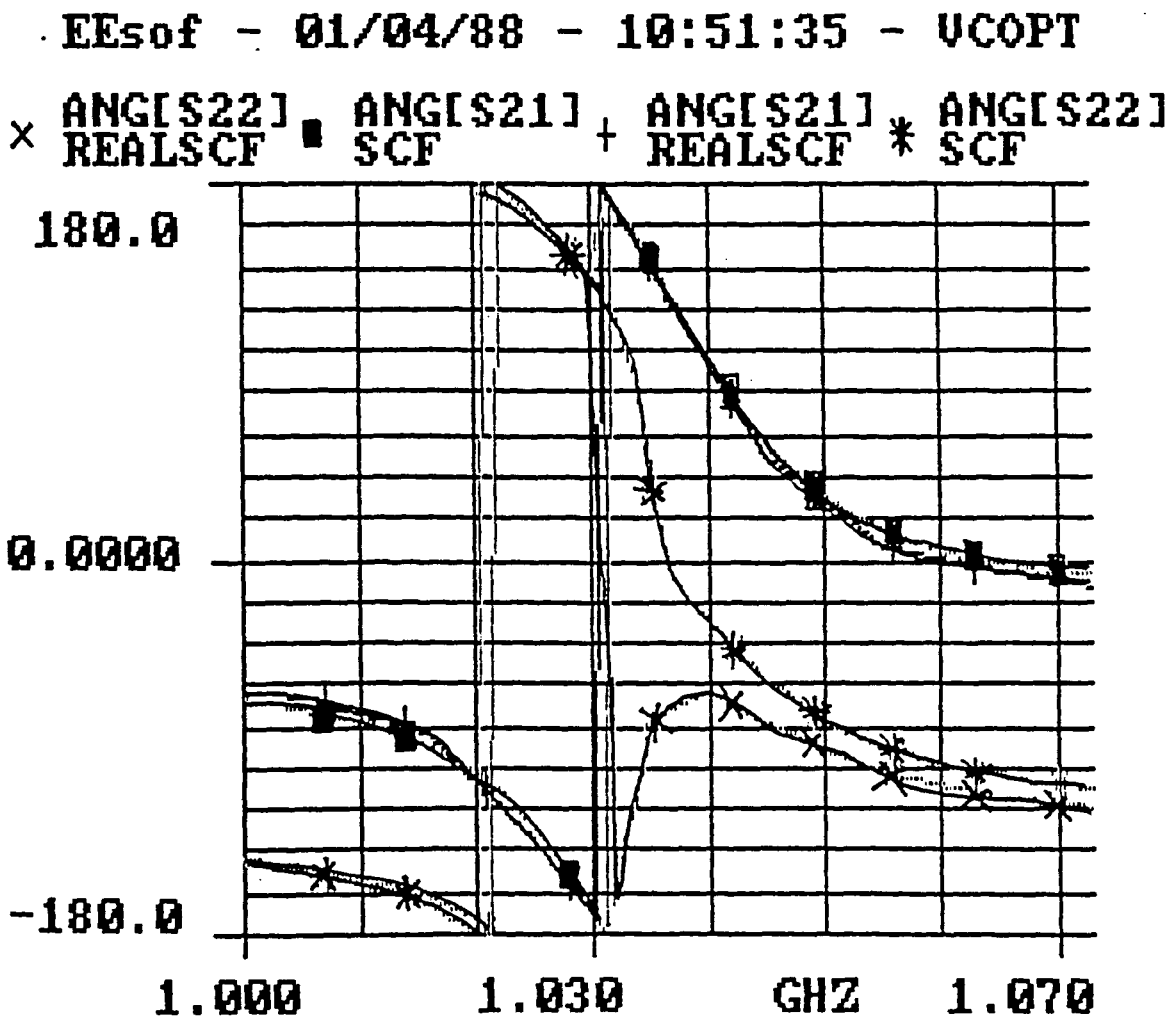


Fig. 4.3b
Phase Plot of Measured (REALSCF) and Computed (SCF) S_{21} and S_{22}

phase slope of S_{21}, which is of primary importance in determining the frequency stability and the amount of tuning possible is very well modeled. The insertion loss of this particular filter is defined as $|S_{21}|_{f=fc}$, where f_c is the center frequency of the filter, and was measured on the HP8505 Network Analyzer to be -4.6 dB occurring at 1035.1 MHz. The unloaded Q for the stacked crystal filter, not to be confused with the unloaded Q of an individual resonator, may be measured on a network analyzer where the source and load impedances are matched, and was determined to be 88.06.

In addition to the filter, the other components comprising the VCO were also characterized in terms of their S parameters at f_c and the results are presented in Table 4.3. The full S matrix was measured for the amplifier over a range of input power for various degrees of compression as described in Appendix C. The varactor diode and its bias network were also characterized over a range of bias voltages to determine the amount of phase shift attainable. Fig. 4.4 is a plot of phase shift vs. applied voltage, and indicates a linear range of approximately 3 to 9 volts with a center of approximately 6 volts. The oscillator was designed such that the middle of the diode's tuning range was aligned with the center of the filter's passband. The frequency tunability was predicted by Eq. 4.1 and was determined to be .335 MHz/Volt for a phase slope of 9.75°/MHz for the filter and a phase - voltage slope of 3.27 °/Volt for the series varactor diode.

$$\Delta f/\Delta V = \Delta f/\Delta \phi \times \Delta \phi/\Delta V \qquad (4.1)$$

Table 4.2 Lumped Element Model Values

Element Name	Value	Units
C_{p1}	0.05076	pF
C_{p2}	0.05099	pF
L_{wb1}	1.71227	nH
L_{wb2}	2.08547	nH
R_{met1}	2.70984	Ω
R_{met2}	2.80994	Ω
C_{o1}	3.84476	pF
C_{o1}	3.84476	pF
R_{s1}	10.4219	Ω
R_{s2}	10.4219	Ω
L_{s1}	306.301	nH
L_{s2}	306.301	nH
C_{s1}	0.07905	pF
C_{s2}	0.07905	pF
L_g	0.97770	nH

Table 4.3 S Parameter Values at 1035 MHz

Component	S_{11} dB @ °	S_{12} dB @ °	S_{21} dB @ °	S_{22} dB @ °
Splitter	-9.542 @ 90	-3.522 @ -90	-3.522 @ -90	-9.542 @ 90
Varactor	-9.4 @ -140	-0.60 @ -56	-0.70 @ -57	-9.4 @ -154
Amp (comp)				
0 dB	-19.7 @ 107	-18.9 @ 49	15.7 @ 96	-17.2 @ 151
0.6 dB	-31.1 @ 71	-17.6 @ 49	15.1 @ 98	-18.1 @ 181
3.8 dB	-12.7 @ -50	-14.2 @ 54	11.9 @ 104	-5.4 @ -34
7.3 dB	-9.5 @ -48	-13.1 @ 54	8.4 @ 101	-4.3 @ -34

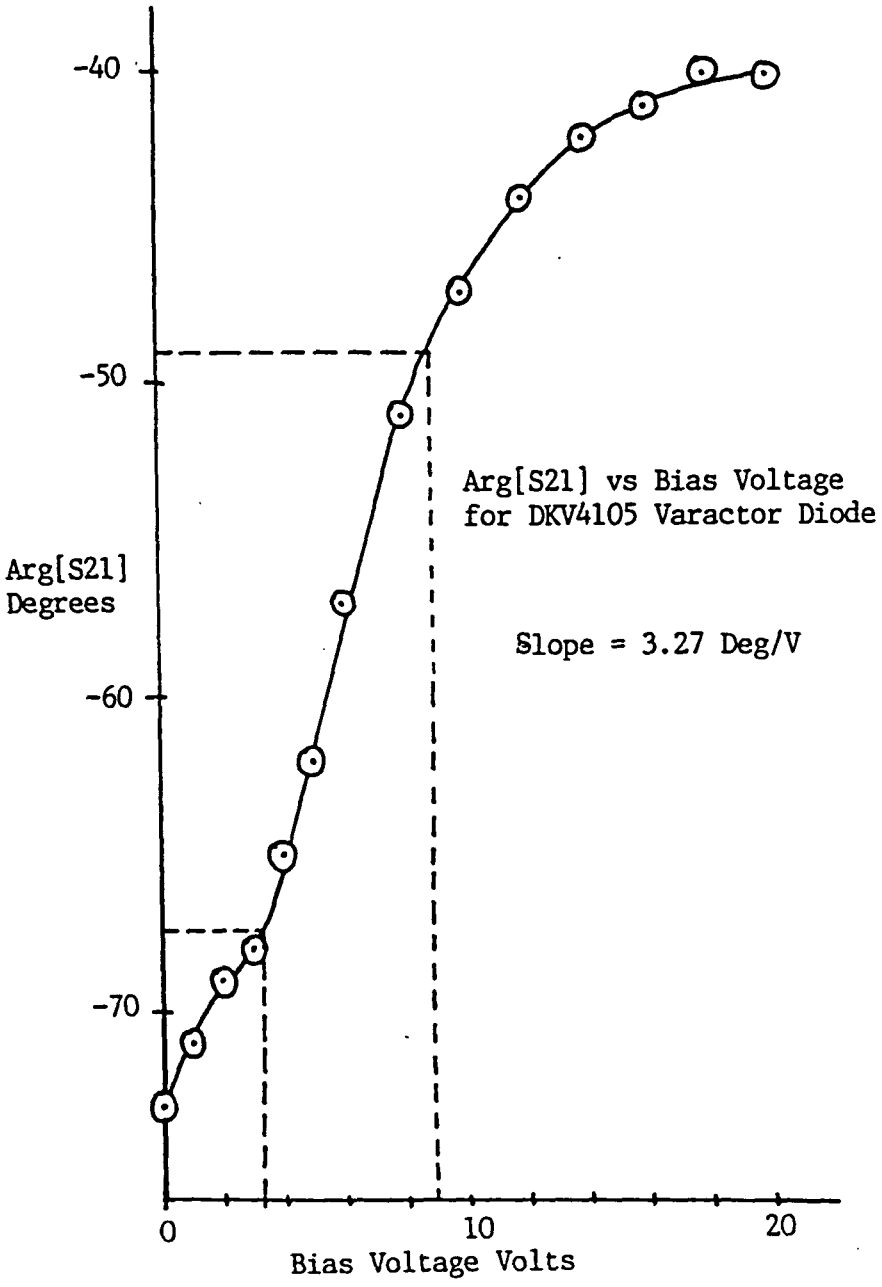


Fig. 4.4
Varactor Tuning Curve

The maximum tuning range was likewise determined from the maximum phase deviation obtainable from the varactor diode over a range of 15 V and was calculated to be 3.18 MHz. The actual tuning slope and the tuning range was expected to be greater in the closed loop circuit since the loaded Q of the filter, which is proportional to the phase slope of the filter, decreases when the loop is closed. Finally, the power splitting "T" was also characterized by its S parameter matrix. The individual S matrices were combined in a Touchstone file which is listed in Fig. 4.5a according to the placement of the devices in the actual oscillator circuit and the net two port S matrix was computed. The nonlinear behavior of the amplifier was accounted for by iteratively changing its matrix values until the open loop gain of the net two port approached 1 which would correspond to the degree of compression at which the amplifier would operate. Once this was done, the open loop phase of the network was adjusted by altering the electrical length of the feedback path until it was very close to 0° at 1035 MHz. The resulting output file is shown in Fig. 4.5b. At this point the general condition for oscillation given in Chapter 3 and repeated in Eq. 4.2, was computed for the open loop two port parameters at 1035 MHz and the vector sum of $\Delta S + S_{12} + S_{21}$ was found to equal 1.132 at an angle of 0.7018°.

$$1 = \Delta S + S_{12} + S_{21} \tag{4.2}$$

Output power was predicted to be approximately 10 dBm. by subtracting 3.5 dB from the actual measured saturated output power of the amplifier again assuming an equal power split into two 50Ω loads.

```
Touchstone (TM) -Ver(1.40-Lot 103)-Targ(IBM-PC/AT)-Ser(16678-2619- 1000)
            VCO1.CKT   01/04/88 - 10:15:11

! name :  VCO
! date : 10-20-88  update 11-06-88,
! purpose: PREDICT PARAMTERS TO SUSTAIN OSCILLATION

DIM
  FREQ GHZ
  RES OH
  IND NH
  CAP PF
  LNG MIL

CKT
  S2PA   1  2  0  AMP
  S2PB   2  3  0  TJUNCT
  S2PC   3  4  0 VARACTOR
  S2PD   4  5  0 VCOFILT
  TLIN   5  6       Z=50  E\110  F=1.037
  DEF2P  1  6  VCO
OUT
  VCO    MAG[S11]
  VCO     ANG[S11]
  VCO    MAG[S21]   GR1
  VCO     ANG[S21]  GR3
  VCO    MAG[S12]   GR1
  VCO     ANG[S12]  GR3
  VCO    MAG[S22]


  VCO     ANG[S22]
FREQ
  SWEEP  1.020 1.050 .001
GRID
  RANGE  1.020  1.050  .001
  GR1   -40  10  5
  GR2   -30  -5 0.5
  GR3   -180 180 10
```

Fig. 4.5a
Touchstone Circuit File for Open loop Oscillator

Touchstone (TM) -Ver(1.40-Lot 103)-Targ(IBM-PC/AT)-Ser(16678-2619- 1000)
VCO1.CKT 01/04/88 - 10:16:12

FREQ-GHZ	MAG[S11] VCO	ANG[S11] VCO	MAG[S21] VCO	ANG[S21] VCO	MAG[S12] VCO	ANG[S12] VCO	MAG[S22] VCO	ANG[S22] VCO
1.02000	0.308	-74.504	0.362	112.465	0.037	65.965	0.737	-36.405
1.02100	0.318	-73.452	0.401	107.280	0.041	60.914	0.709	-40.096
1.02200	0.329	-72.568	0.439	102.077	0.045	55.844	0.681	-43.818
1.02300	0.340	-71.839	0.479	96.853	0.049	50.753	0.653	-47.573
1.02400	0.350	-71.256	0.518	91.609	0.054	45.643	0.624	-51.357
1.02500	0.361	-70.806	0.559	86.344	0.058	40.511	0.594	-55.167
1.02600	0.376	-71.110	0.617	78.858	0.063	32.858	0.520	-61.557
1.02700	0.390	-71.513	0.676	71.345	0.069	25.178	0.445	-68.079
1.02800	0.404	-72.010	0.736	63.803	0.075	17.470	0.368	-74.772
1.02900	0.419	-72.594	0.797	56.235	0.081	9.735	0.291	-81.708
1.03000	0.433	-73.259	0.859	48.636	0.087	1.970	0.212	-89.073
1.03100	0.448	-74.157	0.907	38.981	0.092	-7.852	0.171	-50.222
1.03200	0.463	-75.130	0.955	29.294	0.097	-17.706	0.166	-9.096
1.03300	0.478	-76.176	1.003	19.572	0.101	-27.594	0.181	21.796
1.03400	0.493	-77.291	1.053	9.817	0.106	-37.516	0.183	41.912
1.03500	0.507	-78.472	1.102	0.031	0.111	-47.470	0.158	54.012
1.03600	0.493	-82.116	1.086	-10.482	0.110	-57.949	0.189	52.477
1.03700	0.501	-85.941	1.081	-20.993	0.109	-68.427	0.214	53.501
1.03800	0.527	-88.383	1.086	-31.178	0.110	-78.578	0.235	56.631
1.03900	0.562	-88.641	1.095	-40.807	0.111	-88.174	0.256	61.545
1.04000	0.592	-86.849	1.101	-49.839	0.111	-97.172	0.279	67.722
1.04100	0.607	-89.869	1.031	-59.882	0.104	-106.982	0.331	68.860
1.04200	0.615	-93.269	0.955	-70.058	0.097	-116.924	0.389	68.553
1.04300	0.615	-96.932	0.874	-80.306	0.088	-126.939	0.451	67.064
1.04400	0.607	-100.739	0.790	-90.555	0.080	-136.955	0.517	64.703
1.04500	0.590	-104.575	0.703	-100.734	0.071	-146.901	0.582	61.756
1.04600	0.579	-105.888	0.653	-105.487	0.066	-151.620	0.610	59.078
1.04700	0.567	-107.163	0.603	-110.208	0.061	-156.308	0.638	56.356
1.04800	0.553	-108.393	0.553	-114.896	0.056	-160.963	0.665	53.604
1.04900	0.539	-109.570	0.504	-119.547	0.051	-165.580	0.692	50.837
1.05000	0.524	-110.685	0.456	-124.158	0.046	-170.158	0.718	48.065

Fig. 4.5a
Output File for Fig. 4.5a

The lumped parameter model values computed by Touchstone were used to model the SCF in an open loop SPICE simulation of the VCO. Again, a transistor level model was used to predict the behavior of the amplifier. A series diode model was included in the feedback path along with an equivalent dc bias network for the diode. Although the exponent in the equation for calculating the capacitance of a hyperabrupt junction diode is voltage dependent, SPICE diode models require that a constant value be used. An exponent of 0.6 was determined to provide the best possible fit to the measured C - V curve and was used in the analysis. The results shown in Figs. 4.6a through c are for bias voltages of 0, 6, and 25 volts, respectively. The oscillation frequencies were determined at the points where the net phase crossed zero, and values of 1034.4, 1035.3, and 1036.4 MHz were predicted for the above three cases. One readily notices that the passband of the filter is shifted up by a few MHz, and that the phase slope is approximately 12°/MHz. This discrepancy accounted for an increase in the filter's Q of 109.3, and thus a decrease in the tuning range to 2 MHz. The analysis was effective in modeling the voltage variance of the diode, and in the least, was useful in determining the trend toward increasing frequency with an increasing bias voltage.

Initial tests of the VCO indicated that the frequency of oscillation with a 6 Volt bias on the varactor was 2MHz too high, an error of less than .2%. The VCO was trimmed using an open stub tuning section to obtain the desired frequency of 1.035 GHz.

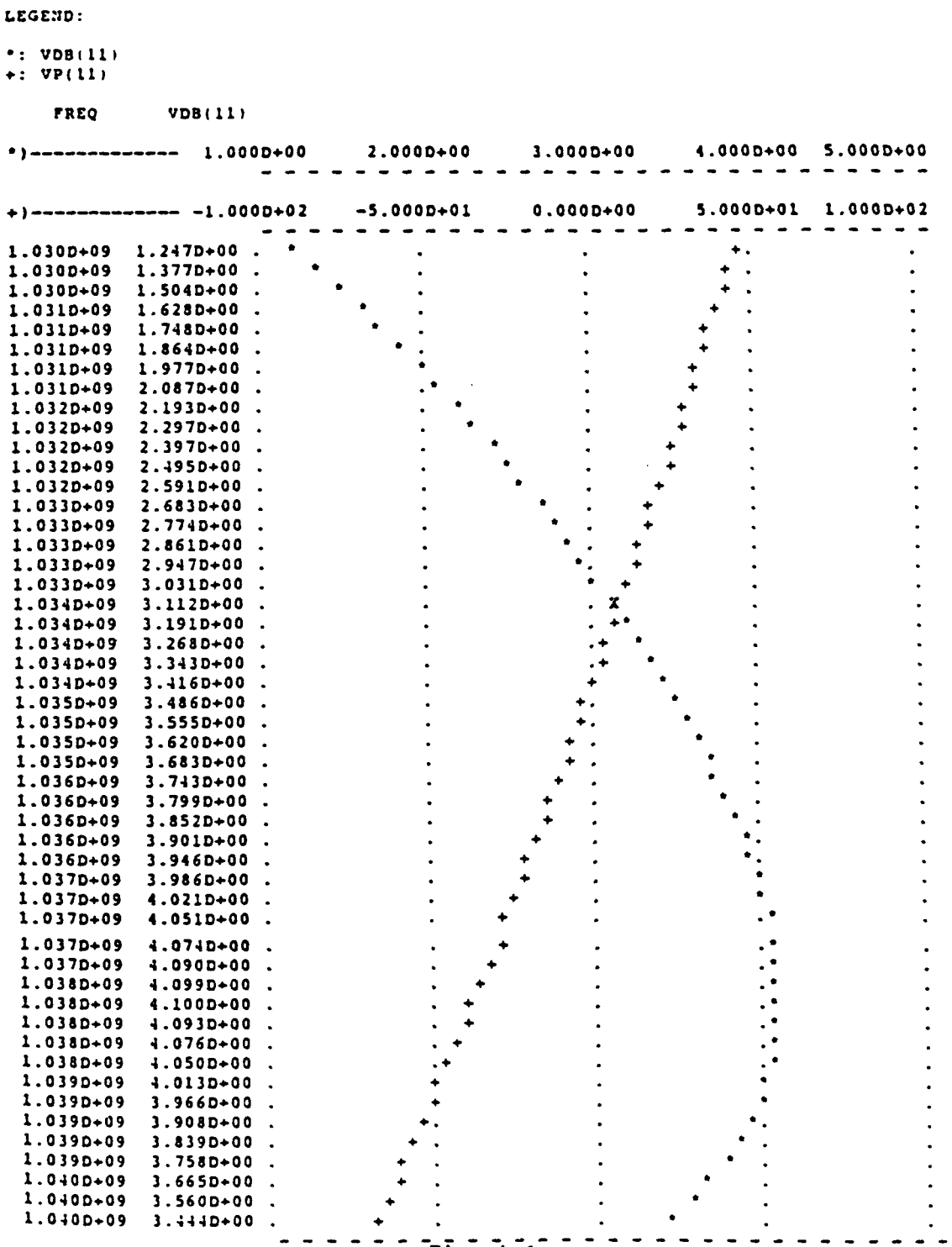


Fig. 4.6a
VCO SPICE Analysis 0 V Bias

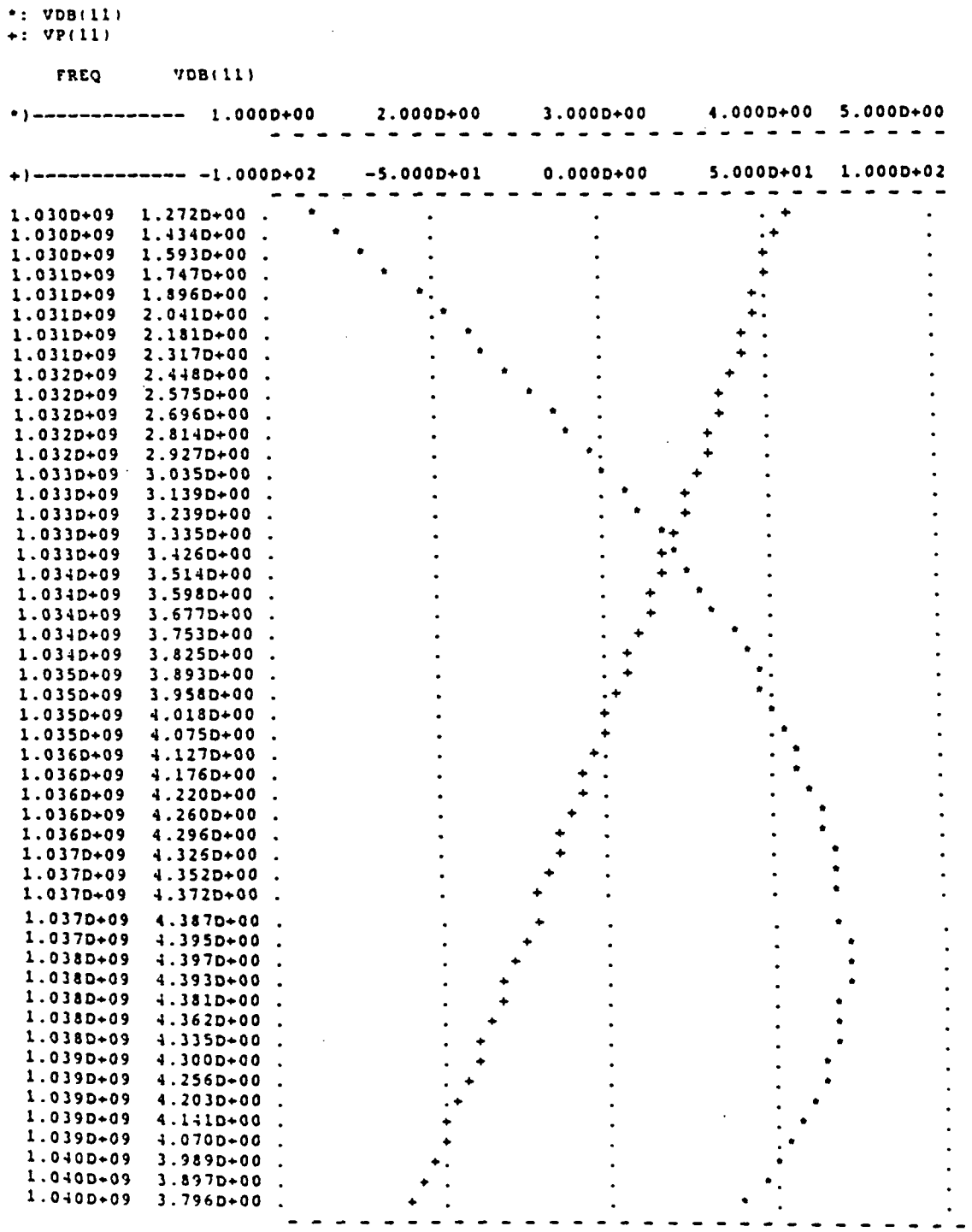


Fig. 4.6b
VCO SPICE Analysis 6 V Bias

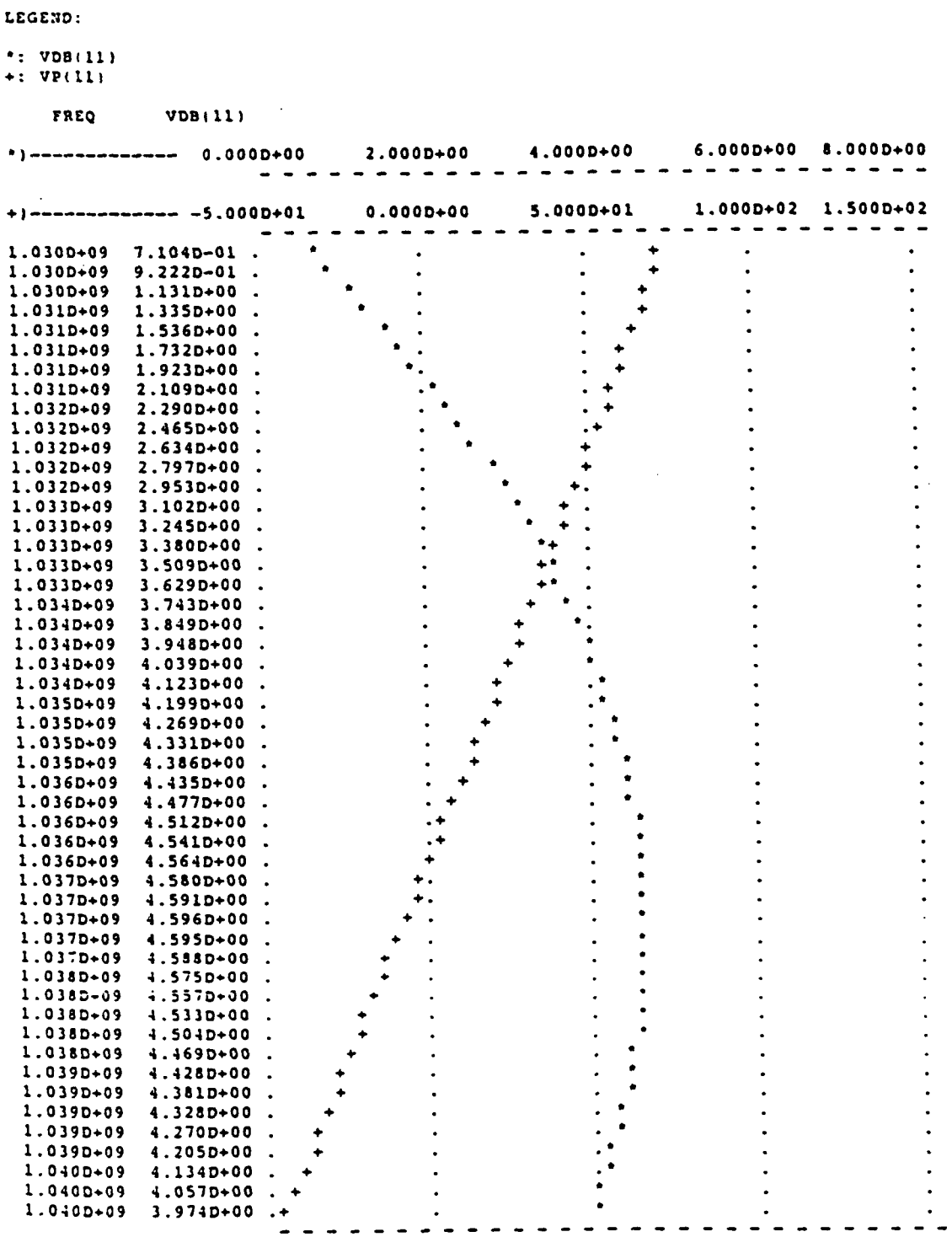


Fig. 4.6c
VCO SPICE Analysis 25 V Bias

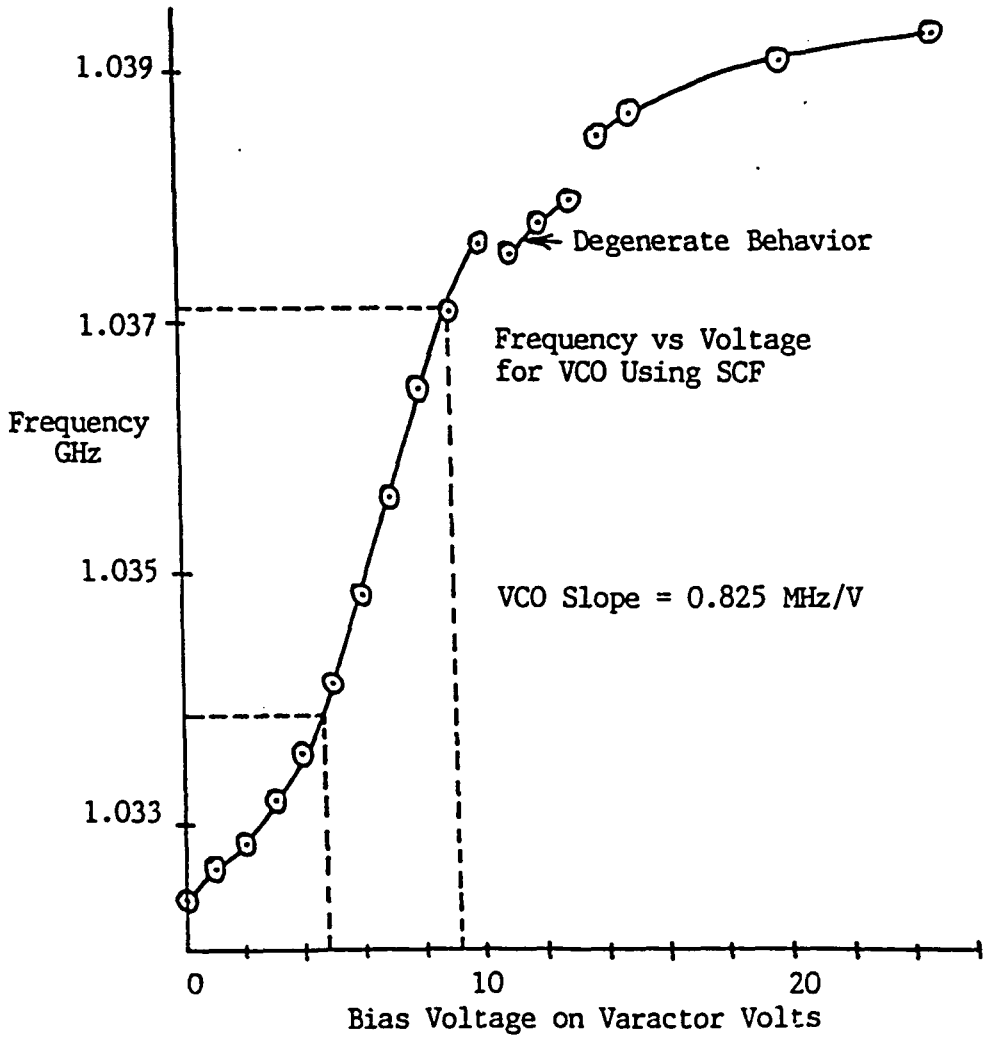


Fig. 4.7
VCO Slope

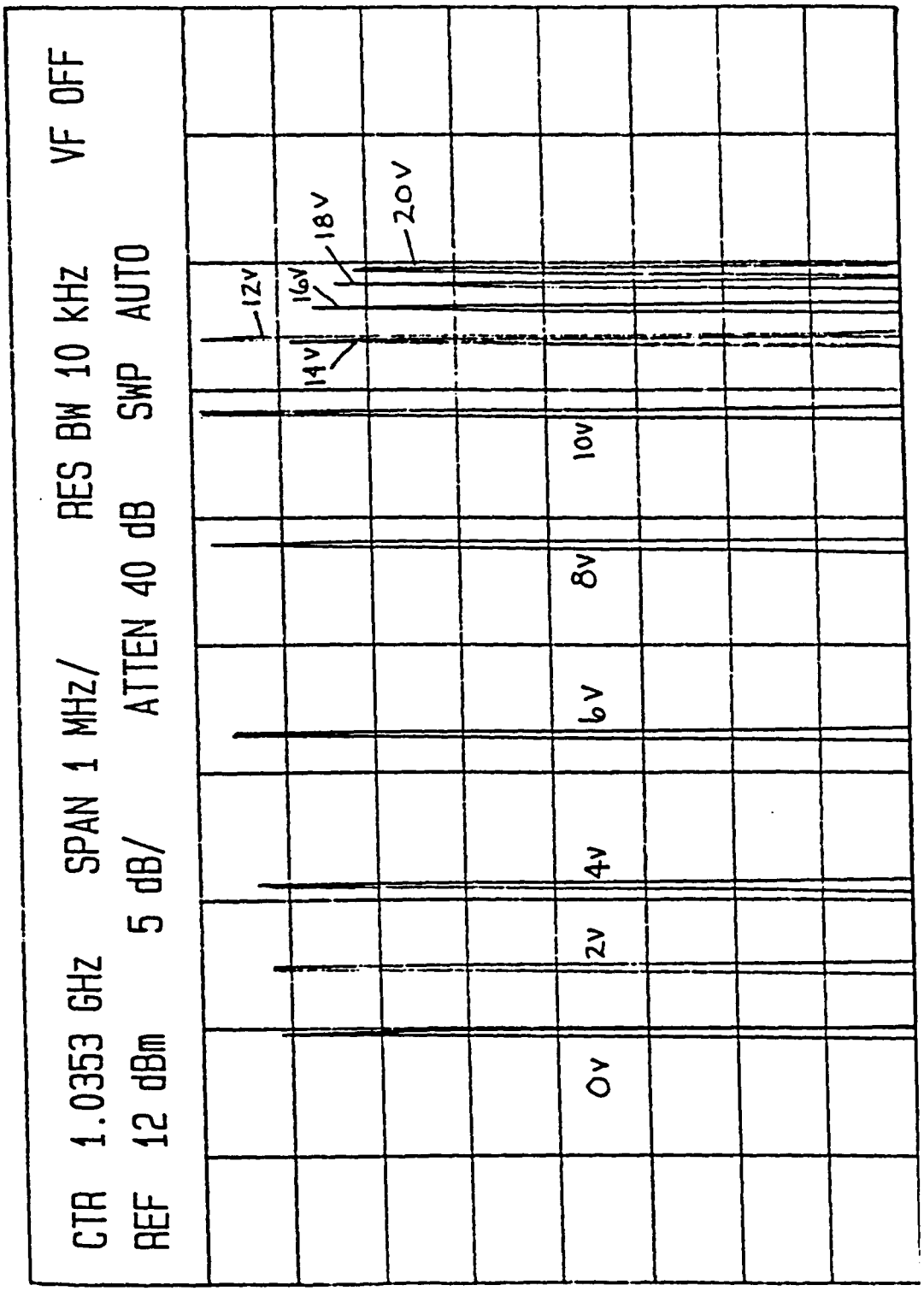


Fig. 4.8
VCO Tuning Plot

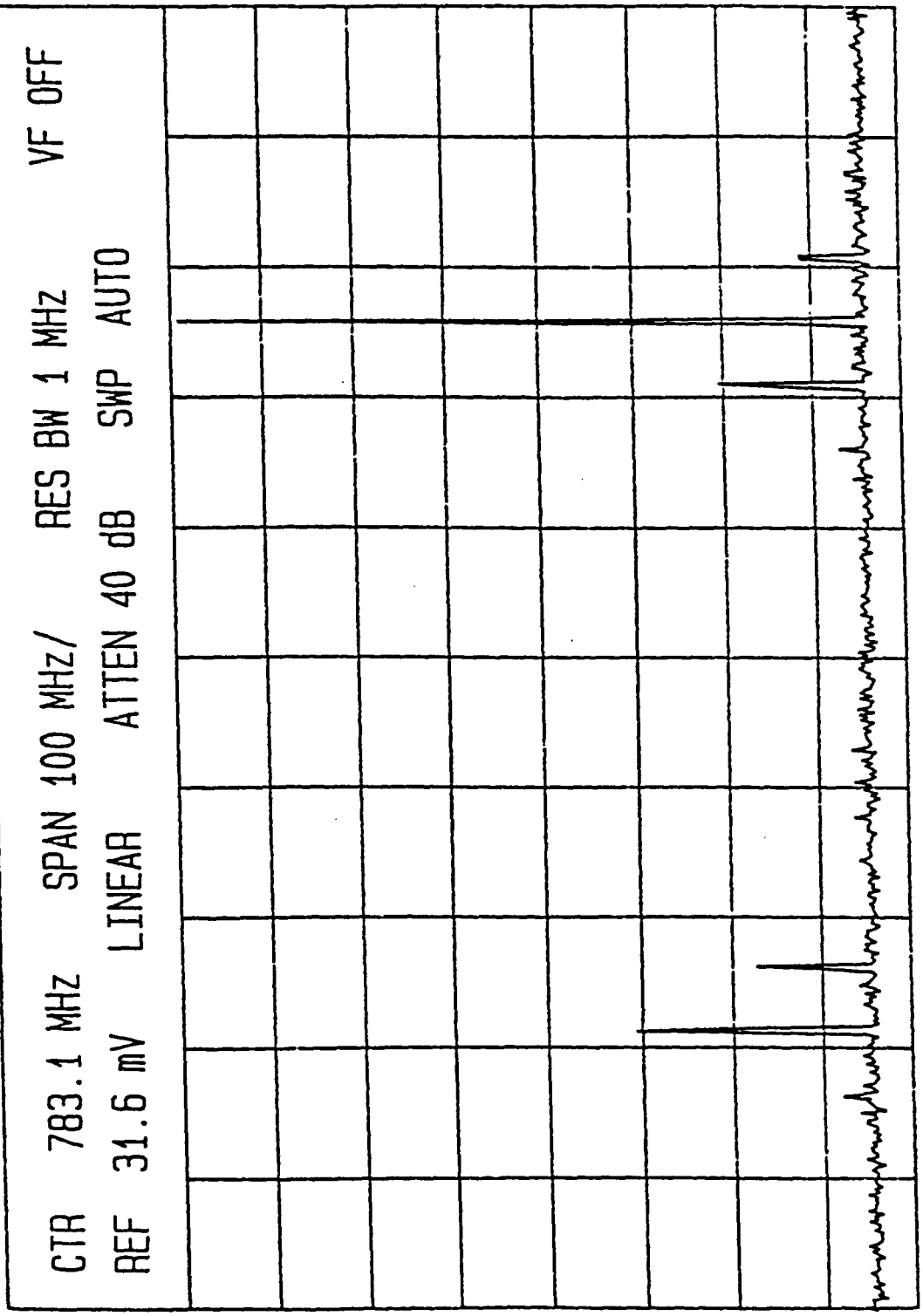


Fig. 4.9
Plot of Degenerate Oscillations

Output power was measured on the HP8569 Spectrum Analyzer as 9.5 dBm which agrees quite closely with the predicted value. The overall tuning range of the VCO was determined to be 5.9 MHz for a range 0 to 20 volts on the varactor and 5 MHz for a range of 0 to 15 volts on the varactor. The VCO slope was plotted as shown in Fig. 4.7 and indicates a maximum slope of .825 MHz/Volt which is higher than that as determined from open loop measurements by a factor of 2.46 which points to a value of Q_L of $Q_{UL}/2.46$ or 35.80. A plot of frequencies corresponding to 2 Volt increments of bias on the varactor is shown in Fig. 4.8. The tuning is seen to be fairly linear in the region of 4 to 9 volts, and outside this range, the tuning becomes compressed due to the nonlinear phase - voltage relation of the varactor as evidenced in Fig. 4.4. Therefore the useable tuning range is reduced to approximately 4 MHz.

The VCO exhibited a degenerate behavior at bias voltages greater than 11 Volts as seen in Figs. 4.7 and 4.8. This is a result of the oscillator operating at the fundamental mode and half order mode which is also supported by the SCF structure. A wideband spectral plot, Fig. 4.9, verifies this as oscillations are seen to occur at 1.037 GHz and approximately 500 MHz. Although undesirable, this behavior occurs only outside the usable tuning range of the VCO. To alleviate this problem, the amplifier could be bandlimited to the frequency range of the fundamental mode.

Another area of concern in oscillator performance is the generation of harmonics. Figs. 4.10a, b, and c are the narrowband spectrum analyzer plots of the fundamental, and second and third harmonics

respectively, with a 0 V bias applied to the varactor, where the latter two are seen to be roughly 30 and 47 dB down with respect to the fundamental which is an improvement over the simple oscillator. Again, bandlimiting the amplifier would decrease the harmonic generation, especially the second which is amplified within the 2 GHz bandwidth of the amplifier used. A summary of the actual VCO performance and comparisons with the predicted performance is given in Table 4.4.

Table 4.4 VCO Performance and Comparisons

Parameter	Predicted	SPICE Simulation	Measured	Units
f_o (6 V)	1035.0	1035.3	1037.1	MHz
Output Power	10.0	-	9.5	dBm
Tuning Range	3.18	2.0	5.9	MHz
VCO Slope	0.335	-	0.825	MHz/V
Stability	-	-	1	ppm
Q_L	88.06	109.3	35.80	-
2nd Harmonic	-	-	-30	dB
3rd Harmonic	-	-	-47	dB

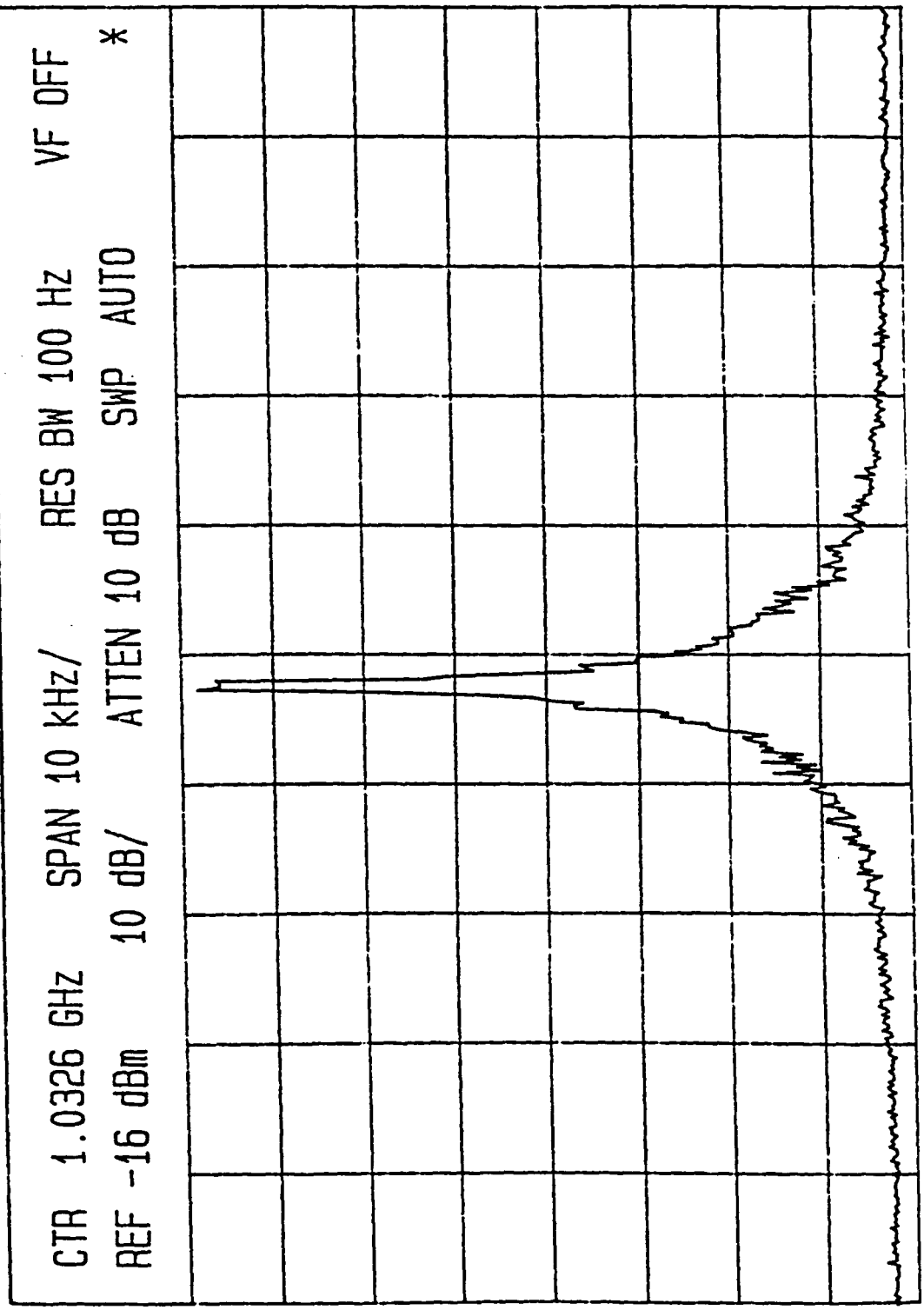


Fig. 4.10a
Plot of VCO Fundamental

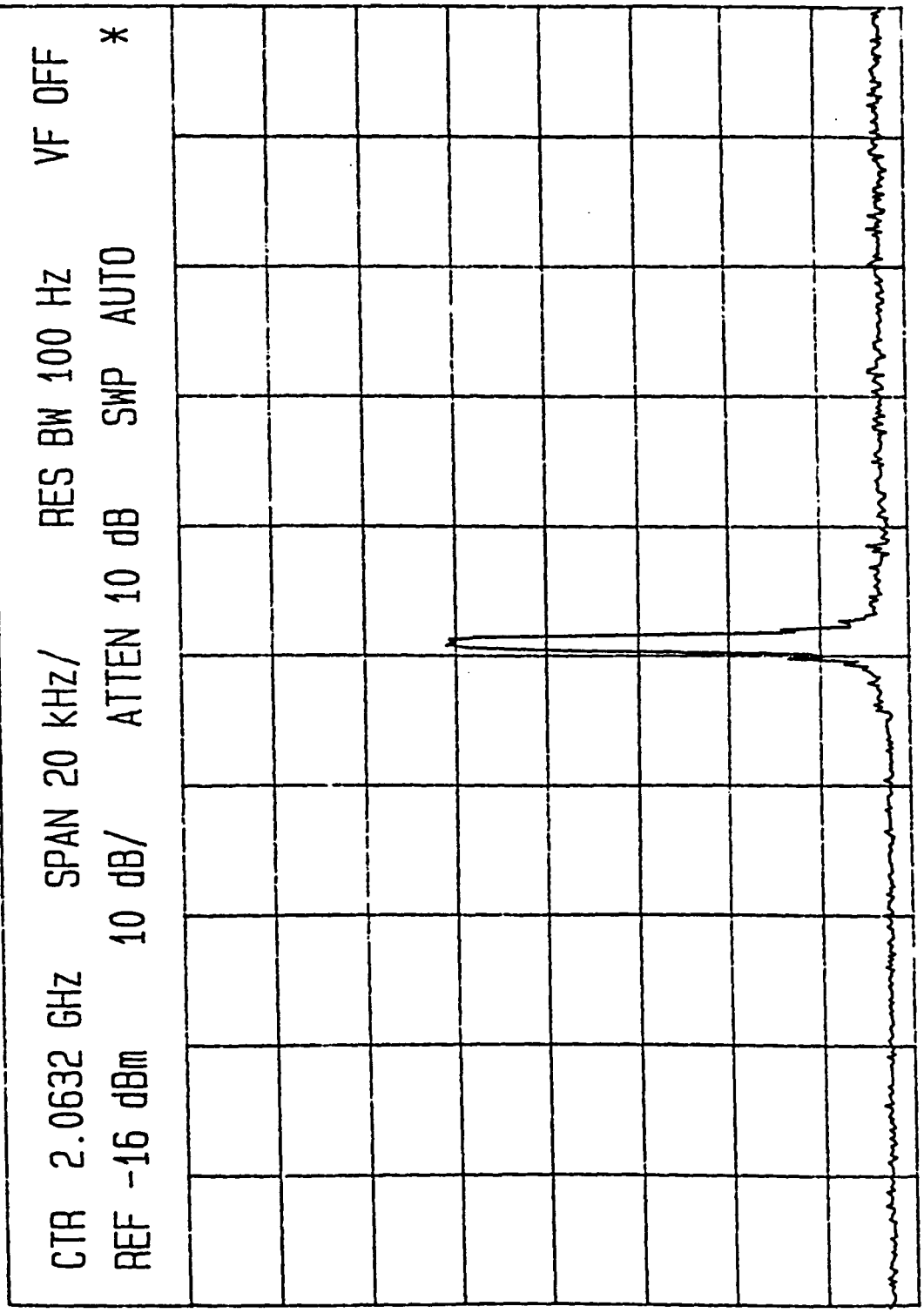


Fig. 4.10b
Plot of VCO 2nd Harmonic

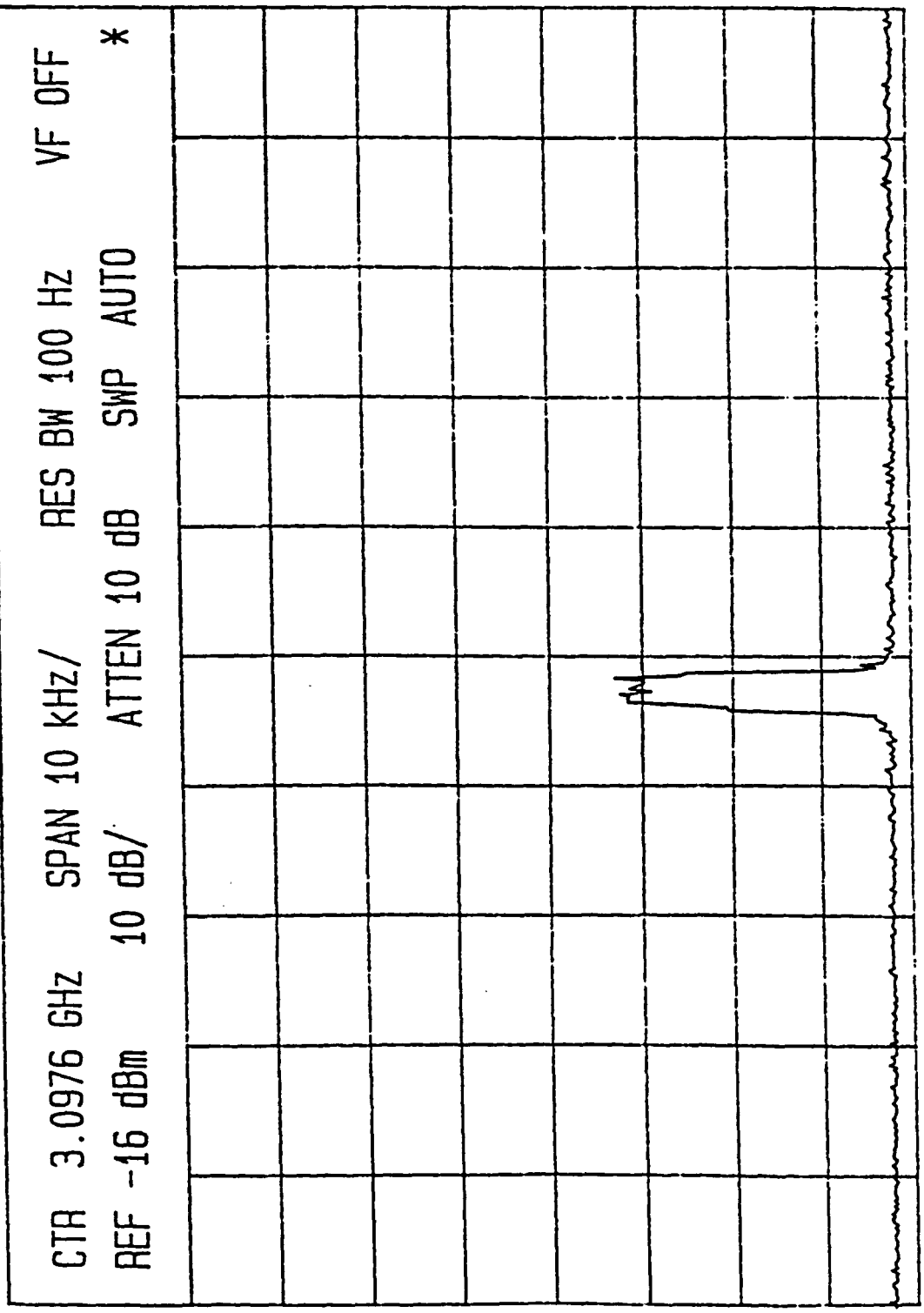


Fig. 4.10c
Plot of VCO 3rd Harmonic

4.3. Frequency Stability

The stability of an oscillator may be defined in three ways: long term stability; the measure of an oscillators frequency fluctuations due to and aging effects measured in terms of months or years, short term stability; the frequency fluctuations as measured in time intervals of a second or so, and phase noise; the frequency or phase deviations occurring in time intervals of less than one second which is more conveniently observed in the frequency domain. The short term frequency stability of the VCO was observed and will be commented on in this section.

To achieve a reasonable degree of frequency stability, it is imperative that an oscillator be allowed to warm up and thermally stabilize, and to isolate it from outside influences. Initial observations of the VCO taken minutes after power up and with no thermal insulation or shielding showed frequency fluctuations greater than 20 kHz or 20 ppm. Approximately one hour after power up, the frequency fluctuations were seen to drop to about 10 ppm as seen in Fig. 4.11 where the trace on the spectrum analyzer was plotted for eight samples taken 40 seconds apart. By placing the oscillator in a metal box padded with plastic packing to provide thermal insulation as well as radio frequency interference (RFI) isolation, and allowing a 24 hour period of undisturbed stabilization and by tapping the signal off of the 20 dB port of a dual directional coupler to reduce loading effects of the spectrum analyzer, the frequency fluctuations were seen be less than 1

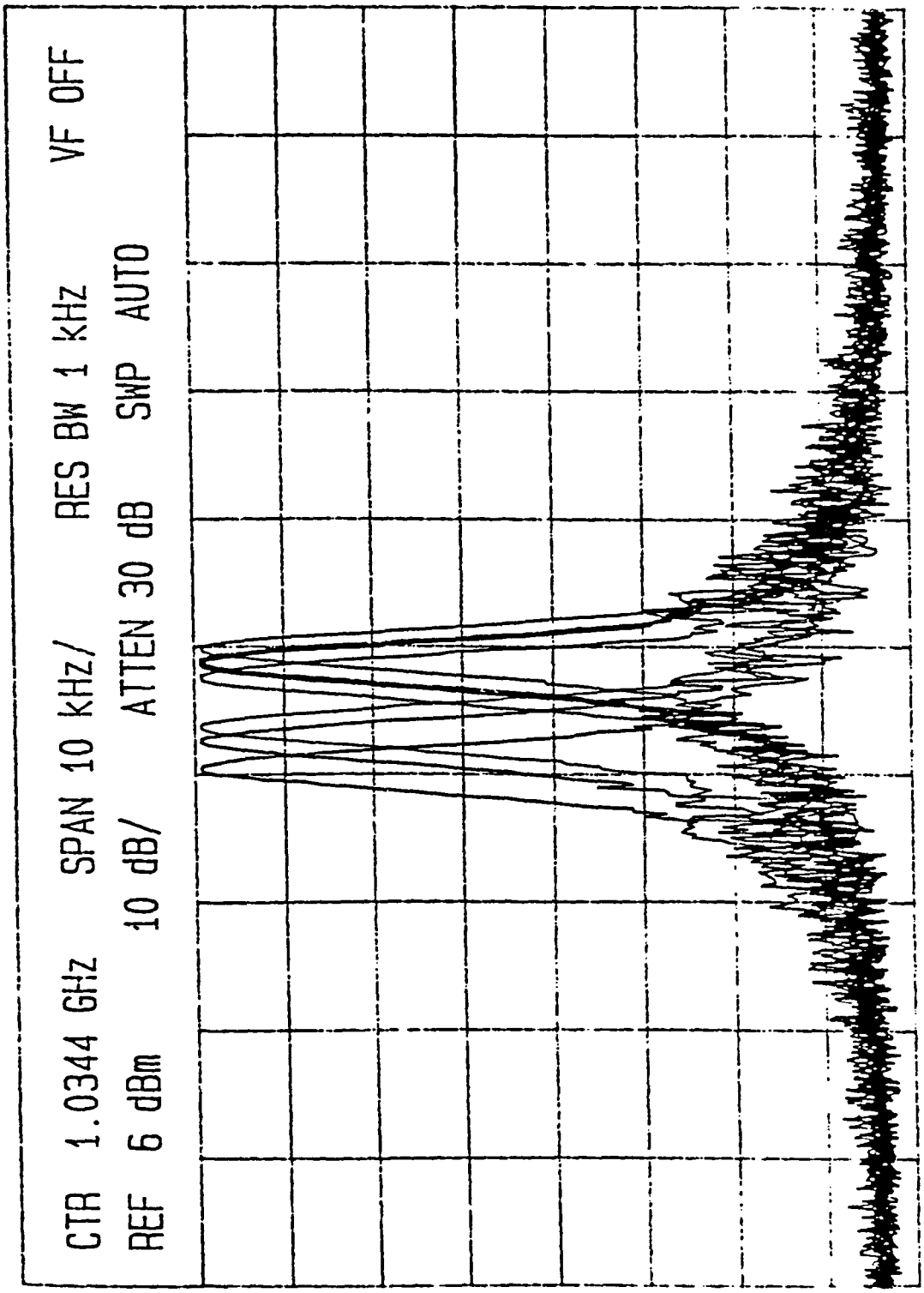


Fig. 4.11
Short Term Frequency Fluctuations

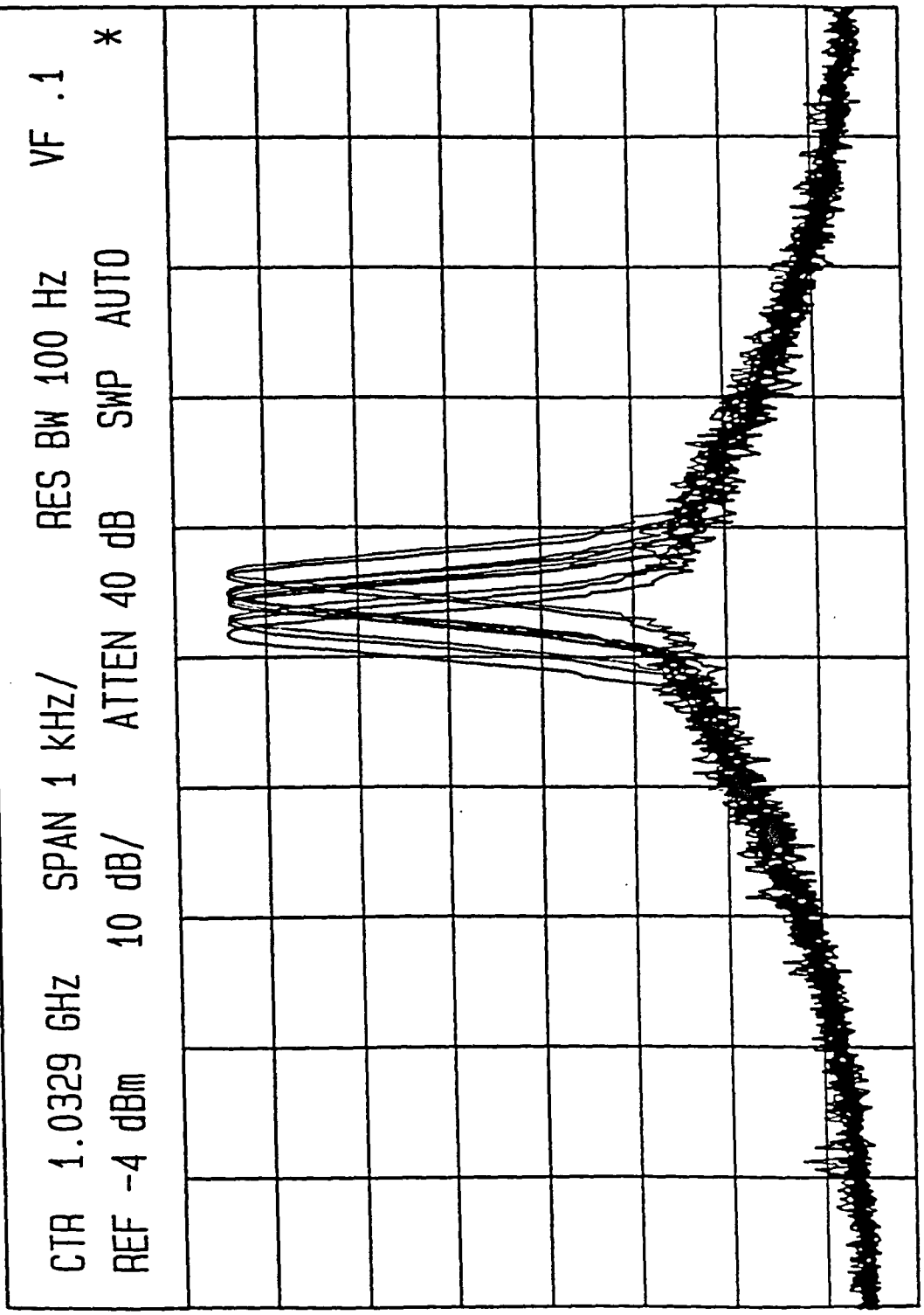


Fig. 4.12
Improved Short Term Frequency Stability

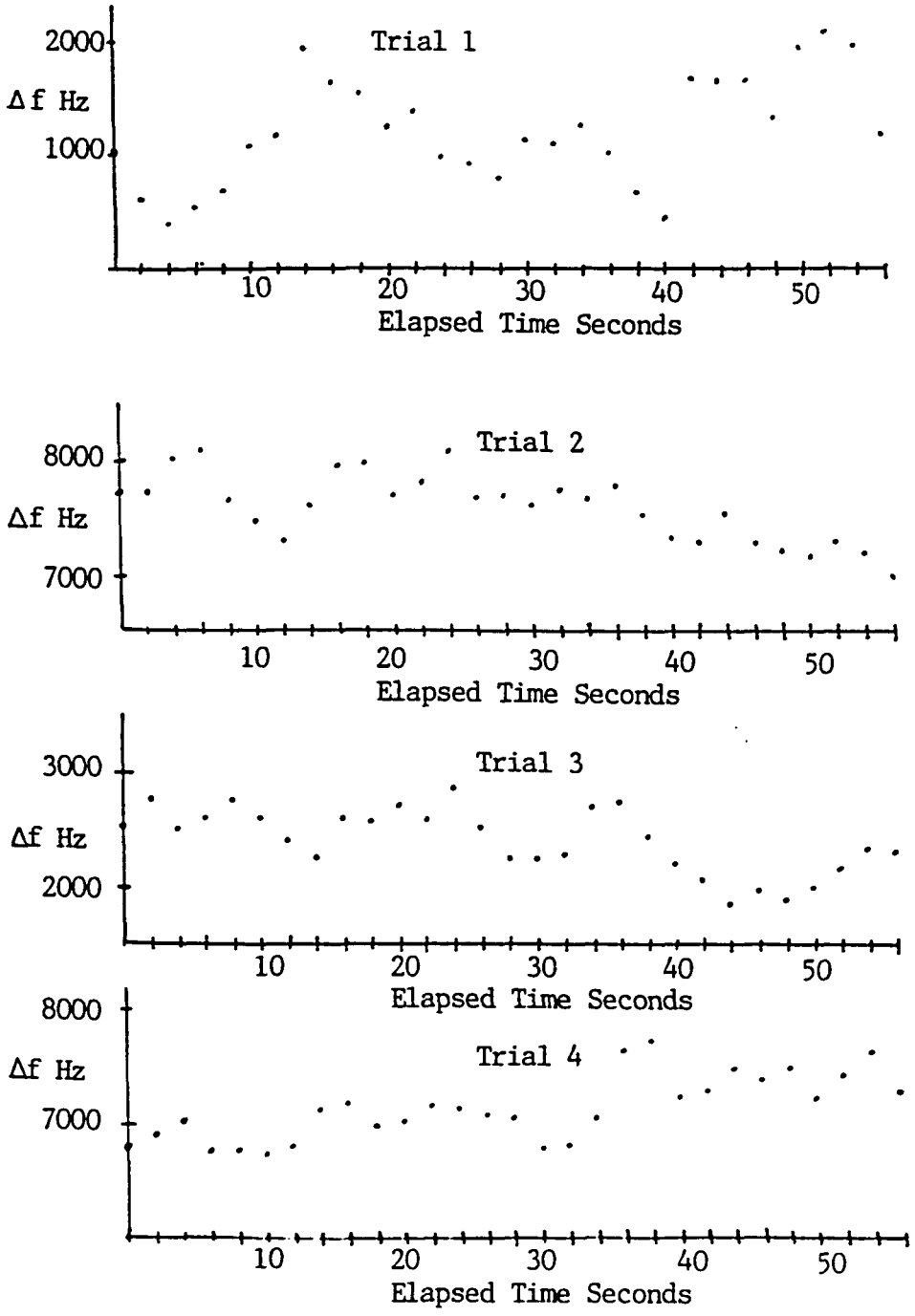


Fig. 4.13
Time Domain Analysis of Short Term Frequency Stability

kHz or < 1ppm measured over a ten minute period with samples traced every 60 seconds as seen in Fig. 4.12. In addition to observing the trace on the spectrum analyzer, a sample of the oscillator's output was fed into an HP5340A frequency counter and readings were recorded at 2 second intervals for four separate trials taken an hour apart as shown in Fig. 4.13. Measurements in trial one were recorded soon after the frequency counter was connected and indicates frequency fluctuations of approximately 3 ppm. The decrease in stability is most likely due to the slight loading change to the oscillator caused by the counter. One hour later the fluctations seem to be confined to a range of 1 kHz. or 1 ppm. and a drifting to a lower frequency is observed. Measurements taken two and three hours later show about the same relative degree of stability, and again some drift is apparent. It seems that the insulation and isolation have helped to reduce the effects of outside influences but the oscillator still exhibits a degree of drift in frequency which may be due to the ambient temperature of the room changing over the course of an hour.

For the purposes of providing a reference frequency for communications applications, frequency stability on the order of 1 ppm is far from optimal. Typically a very stable, temperature compensated oscillator would be used to provide such a signal. The performance of the VCO is typical of free running oscillators at this frequency and may be dramatically improved by phase locking the VCO to a more stable source.

4.4. VCO Applications

The applications of a Phase locked loop (PLL) are numerous and include tracking an incoming signal, improving the noise performance of a reference source, and demodulating FM signals. VCO operation is also necessary when phase noise measurements are made as discussed in Chapter 5. The block diagram for a PLL is shown in Fig. 4.14 where the VCO is seen to be an essential component. PLL operation was demonstrated using the TFR based VCO by locking it to the HP8662 frequency synthesizer as a reference and using the HP3047 phase noise measurement system to provide the phase detector and control voltage functions of Fig. 4.14. Calculation of the VCO slope and center of tuning voltage are necessary parameters for the system to lock the VCO to the reference and were readily available from earlier measurements of the VCO performance. Under voltage control, a sample of the VCO's output was fed into the counter where the frequency now exhibited no deviation down to 1 Hz, the maximum resolution of the counter. Lock was achievable for frequencies of 1035.5 MHz ± 1 MHz. The phase noise performance of the PLL will be discussed in detail in Chapter 5.

The VCO was also used to demonstrate direct single frequency - frequency modulation (SFFM) by biasing the varactor diode with a DC voltage of 6 volts to allow for the best possible linearity, and applying an ac signal of 50 kHz on the varactor using the HP8662 source. When a carrier is modulated with a single frequency (f_m), the waveform in the frequency domain consists of the carrier and sideband components symmetrically spaced about the carrier at intervals of f_m. The relative

sideband levels may be computed using Bessel functions, where the argument of the Bessel function (β) is referred to as the index of modulation and is proportional to the modulating signal amplitude and inversely proportional to f_m. The unmodulated carrier was observed to determine its amplitude for the purposes of normalization. The modulating signal was then increased until the carrier nulled out corresponding to the first zero of J_0 and a modulation index of 2.4 as shown in Fig. 4.15. Sideband levels were measured and normalized. The modulating signal level was further increased until a second null was observed corresponding to the second zero of J_0 and a modulation index of 5.5 as shown in Fig. 4.16. Sideband levels were again measured and normalized. Results for an index of modulation of 2.4 and 5.5 and the tabulated theoretical values are shown in Table 4.5 for the purpose of comparison where the results are seen to agree well with the theory [18].

Table 4.5 SFFM Results and Comparisons

Value	β = 2.4	J_0	J_1	J_2
Tabulated		.00250	.52018	.43098
Measured		0	.52019	.43132
Deviation		-	-	4.13%
	β = 5.5			
Tabulated		.00684	.34143	.11731
Measured		0	.32830	.12673
Deviation		-	3.84%	8.03%

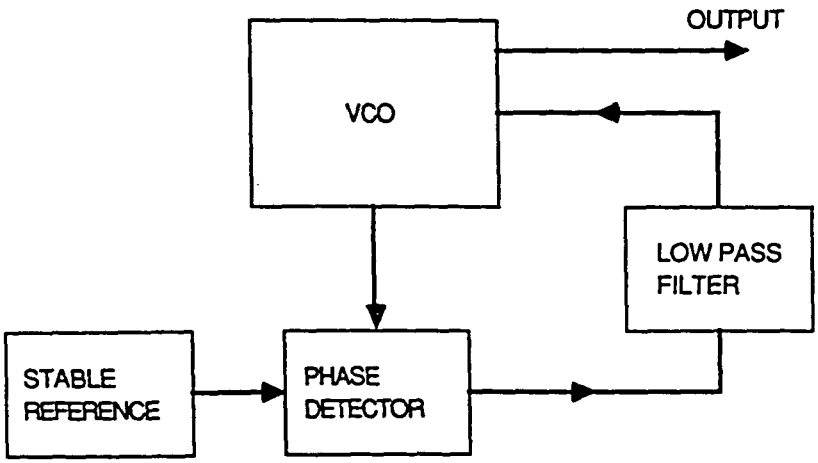


Fig. 4.14
PLL Block Diagram

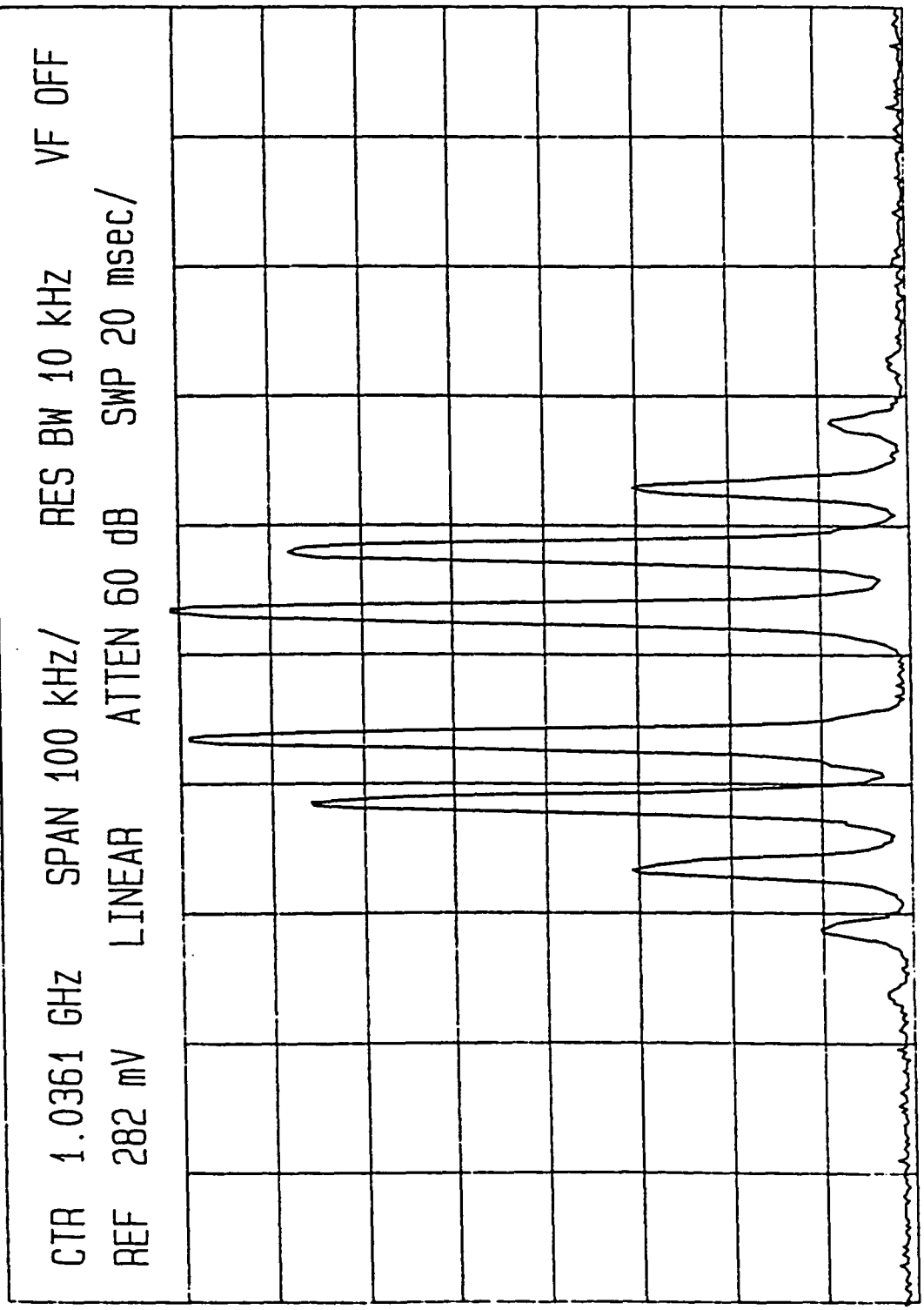


Fig. 4.15
SFFM Plot β = 2.4

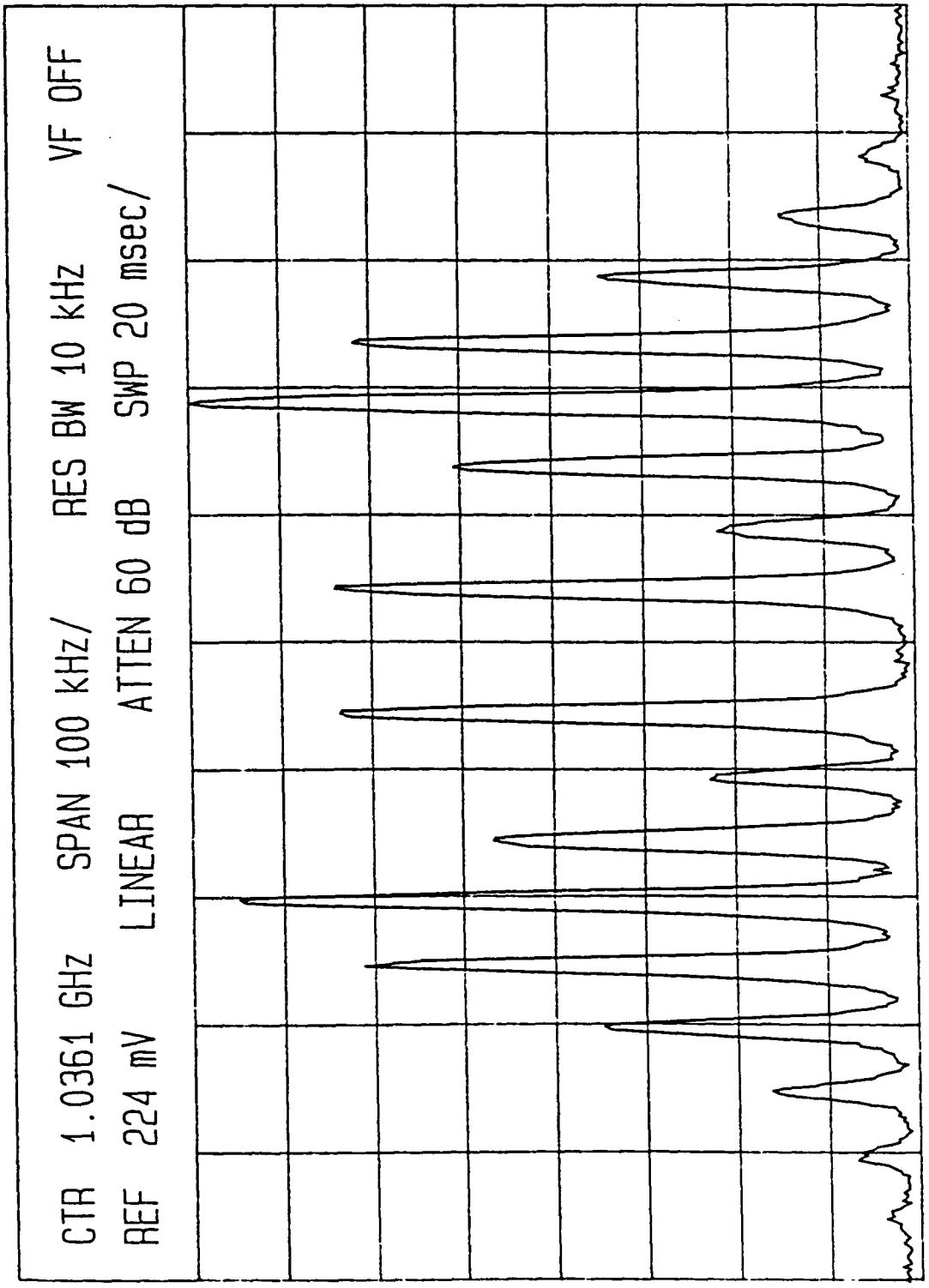


Fig. 4.16
SFFM Plot β = 5.5

4.5. Overmoded Filter Design Example

The final design example is that of a frequency selectable low noise oscillator employing an overmoded stacked crystal filter in the feedback network as described in Chapter 3. The LNA of the HP11729 was used to provide gain to the circuit and a variable attenuator was included to prevent the LNA from being driven into compression. The remainder of the circuit was constructed in a similar manner to those reported on in reference 4, with the inclusion of a second filter, a series stacked crystal filter, in series with the overmoded device in order to allow one mode to be satisfied at a time. The series combination was measured open loop on the HP8505 and the responses of $|S_{21}|$ and $\arg\{S_{21}\}$ were shown in Fig. 3.13 of Chapter 3. The maximum magnitude responses occur at 1030.4, 1034.8, and 1039.2 MHz. These responses correspond to the maximum phase slopes of the three modes where Q_{UL} is roughly estimated to be 2400. It should be noted that the frequency resolution of the network analyzer is not sufficient to make accurate measurements on filters with Q values of this magnitude. The oscillator was constructed and the line stretcher adjusted until a single response at 1039.2 MHz. was observed on the spectrum analyzer. A provision for a small degree of tuning was accomplished by including a varactor diode in series with the two filters. Short term frequency fluctuations were observed to be on the order of .1 ppm with no provision for thermal isolation.

The output of the oscillator was predicted to be 4.5 dBm by subtracting 5.5 dB, the loss in the HP11652 Power Splitter, from the 10

dBm maximum output of the HP 11729 LNA. Measured power at 1032.4, 1034.8, and 1039.2 MHz was 5.0 dB, with the amplitude remaining constant throughout the tuning range of each mode. This illustrates the superior amplitude control of the LNA for various loading conditions which eliminates AM modulation of the carrier.

The VCO slope was measured by biasing the varactor at 6 volts and centering the tuning curve of the varactor, using the line stretcher, at 1039.05, 1039.10, 1039.15, and 1039.20 MHz. Measurements of the VCO slope were determined to be 25.55 kHz/volt, 15.30 kHz/volt, 9.80 kHz/volt, and 10.05 kHz/volt respectively. This indicates that the minimum VCO slope, and hence the maximum Q_L occurs between 1039.15 and 1039.20 MHz. At 1039.15 MHz, Q_L was calculated to be 3025 using a varactor tuning slope of 3.27 °/volt and the VCO slope plot of Fig. 4.17.

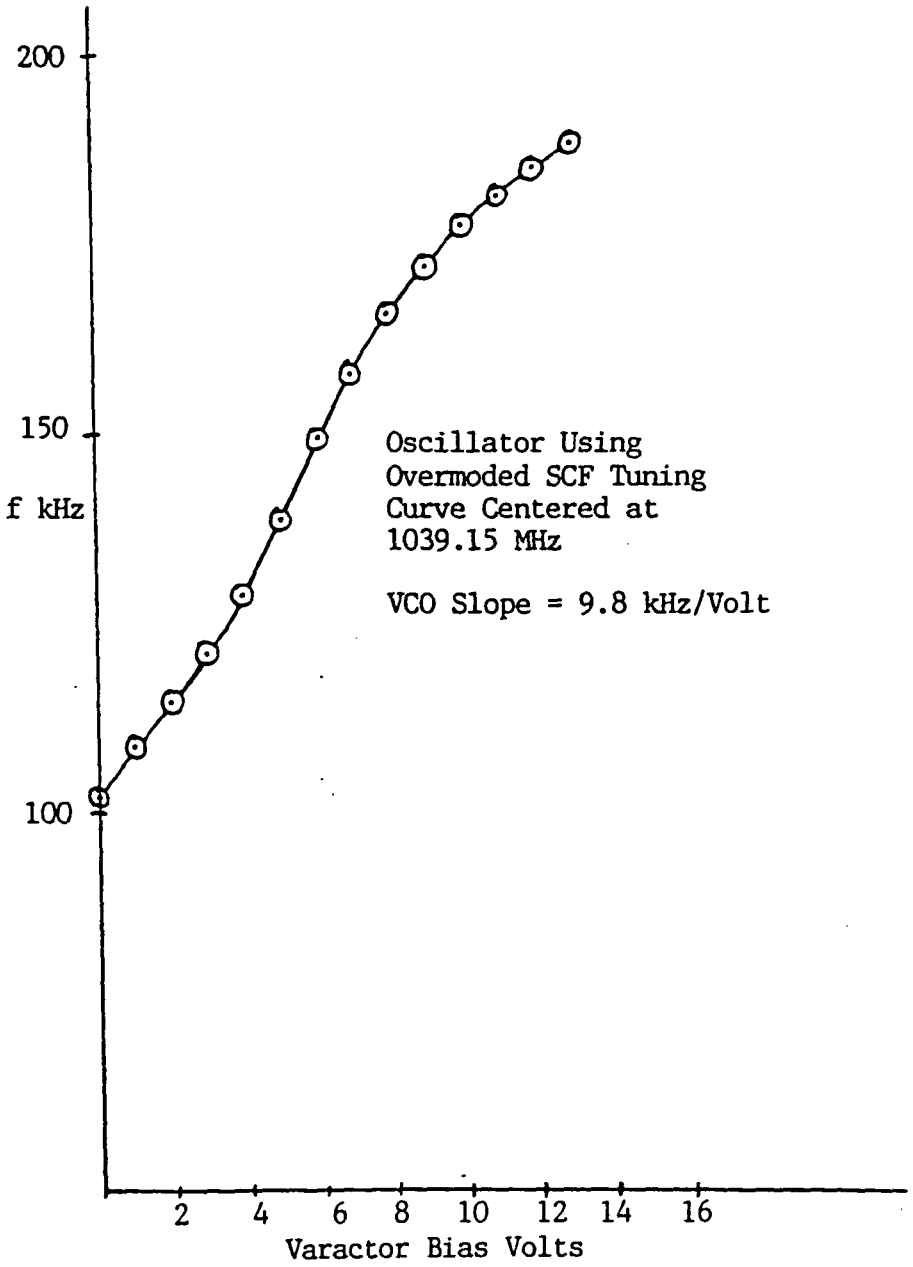


Fig. 4.17
Plot of VCO Slope

5. NOISE ANALYSIS

5.1. Noise Overview

Noise is an inherent phenomenon in any oscillator. Indeed, the basic premise of oscillator operation involves reinforcing the noise components at a desired frequency and rejecting all others. An ideal oscillator spectrum would appear as an impulse function in the frequency domain. The corresponding feedback network would have zero bandwidth and infinite Q. In reality, all sources contain sidebands or spectral content at frequencies offset from the carrier. The amount of power contained in the sidebands with respect to the carrier frequency is a determination of spectral purity or phase noise.

The noise in an oscillator consists of amplitude modulated (AM), and frequency (FM) or phase modulated (PM) components. They exist simultaneously since the changes in the amplitude characteristics of the feedback network generally correspond to changes in the phase characteristics, so that one form of modulation creates the other. However, AM modulation can more easily be eliminated by passing the output of the oscillator through a limiter and is therefore not a serious concern. Noise components may be further described as deterministic, the result of discrete sources such as power lines, RFI, etc., or random. The primary area of concern is with the random noise components since the deterministic sources are more easily identifiable and therefore easier to eliminate. Phase noise may be described as the result of the inherent nonlinearity of the oscillator where noise

components intermodulate with each other and also with the carrier. This also explains the origins of higher order harmonic content [6, p. 47]. Since an oscillator's feedback network has a finite Q and thus a nonzero bandwidth, the noise components at small offset frequencies from the carrier and their modulation products within the bandwidth of the feedback network are of concern as are low frequency noise components due to flicker effects in the active device and the resonator or filter which also modulate the carrier. Neglecting flicker and random walk effects for the time being, the absolute noise floor for an oscillator may be determined from an analysis of thermal or white noise. Outside the bandwidth of the feedback network, the noise would be constant with frequency as the term white noise implies. However, close to the carrier, these components are reinforced by the positive feedback of the oscillator circuit. Within the bandwidth of the feedback network, Eq. 5.1 may be used to calculate the phase noise density in a 1 Hz. bandwidth with respect to the carrier

$$\frac{P_{sb}}{C} = \frac{FkT\ f_o^2}{8CQ_L^2 f_m^2} \tag{5.1}$$

where C is the power in the carrier, F is the noise figure of the amplifier, Q_L is the loaded Q of the feedback network, f_o is the carrier frequency, and f_m is the frequency offset from the carrier [6, p. 53]. One observes that this type of noise follows a $1/f^2$ law and is dependent on the loaded Q as $1/Q_L^2$. It is for this reason that high performance oscillators employ resonators that have high values of Q. It also

explains why high frequency oscillators are noisier than lower frequency ones due to the f_o^2 dependence.

Frequency fluctuations or phase noise may be quantified in a number of ways. In the time domain, it may be described by an Allen Variance, and more commonly, in the frequency domain it may be described by the spectral density of frequency fluctuations ($S_{\Delta F}$), the spectral density of phase fluctuations (S_ϕ), or most commonly the single sideband noise to carrier ratio (L(f)). The above are related as follows:

$$S_\phi(f) = S_{\Delta F}(f)/f_o^2, \tag{5.2}$$

if $S_\phi(f) << 1$ then this parameter may be interpreted as the double sideband noise to carrier ratio of phase fluctuations and

$$L(f) = 10\ \mathrm{Log}(S_\phi(f)/2). \tag{5.3}$$

In the general case where flicker effects as well as other noise sources are considered, the phase noise may consist of various power laws of f^{-n} as illustrated in Fig. 5.1 [19]. A feedback model of an oscillator was used to describe the f^0 through f^{-3} noise components by Leeson as presented in Eq. 5.4 where N is the frequency multiplication factor, G is the gain of the amplifier, and α is the flicker noise coefficient of the amplifier, resonator, or both in sec^{-1} [20].

$$\frac{P_{sb}}{C} = 10\ \log\left[N^2 \left\{ \frac{\alpha f_o^2}{8\pi f_m^3 Q_L^2} + \frac{GFkTf_o^2}{8CQ_L^2 f_m^2} + \frac{\alpha}{2\pi f_m} + \frac{GFkT}{C} \right\} \right] \tag{5.4}$$

The first term corresponds to flicker noise within the bandwidth of the

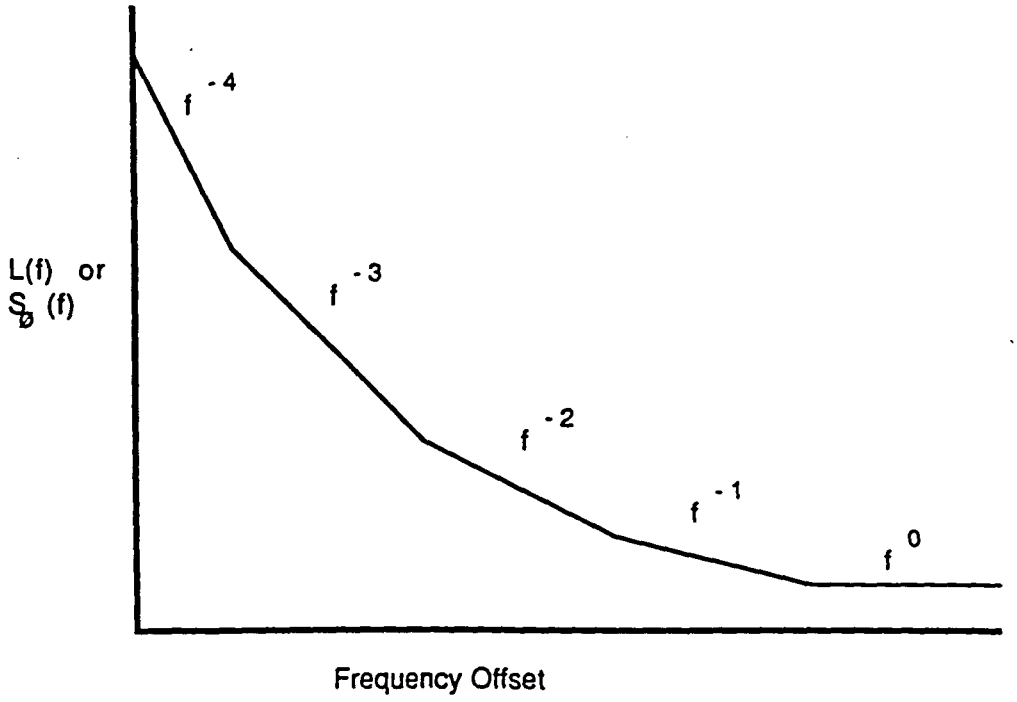


Fig. 5.1
General Oscillator Phase Noise Curve

feedback network, the second term is that of Eq. 5.1 modified to include an amplifier gain greater than unity to overcome the feedback insertion loss, the third term corresponds to the flicker noise present outside of the bandwidth of the feedback network, and the last term describes the absolute noise floor due to thermal noise. The f^{-4} dependence close to the carrier is due to random walk effects and is poorly understood [19].

The effect of phase noise is to reduce the spectral purity of the signal which tends to increase the bandwidth requirements in communications systems. It is therefore desirable to eliminate as much as possible the power in the sidebands of the carrier.

For a given temperature, the thermal noise effects are beyond control. We can choose an amplifier with a low noise figure and reduce the insertion loss in the feedback network as much as possible, so as to reduce G. A resonator or filter with a high Q may be used, although the resonator or filter's insertion loss will increase as Q increases in general [19]. Increasing Q is also considered a tradeoff if tuning of the oscillator is desired.

5.2. Flicker Noise

The flicker effect is a poorly understood noise process, thus making the flicker noise coefficient α, by and large an empirical quantity which may vary between otherwise identical devices. However, certain classes of devices, e.g., GaAs FETs and bipolar transistors, or surface acoustic wave (SAW), bulk acoustic wave (BAW), and dielectric resonator (DRO) resonators do exhibit characteristic values of α. The flicker noise coefficient for the amplifier may also increase as the

amplifier is driven into compression so that this may be a consideration if the flicker noise of the amplifier is playing a dominant role in the noise performance [19].

Open loop measurements of the flicker noise in both the amplifiers used and the resonator based filters were conducted in order to determine the dominant effect. The flicker noise of two port devices may be measured on the HP3047 Phase Noise Measurement System by using the setup illustrated in Fig. 5.2. The error in the system configured in this manner is ± 4 dB [21]. A low noise signal source (HP8662 RF Synthesizer) is fed into a splitter where part of the signal is fed into the LO port of a mixer, and the other feeds power to the DUT. A line stretcher is included between the DUT and the R port of the mixer to establish a condition of quadrature or 90° phase shift between the two signals. This causes any noise components common to both signals to be exactly out of phase by 90° and therefore cancellation occurs. The noise floor of the system is measured by replacing the DUT shown in Fig. 5.2 with a through line. Fig. 5.3 is a plot of the noise floor of the HP3047 at a frequency of 1039 MHz. Components used in constructing the oscillator circuits were systematically tested using this method. Fig. 5.4 is a plot of one of the devices tested, and is typical of the measurements made. One should notice that a 1/f slope is apparent at low frequencies out to the point where the measurement is buried in either the thermal noise of the DUT or the system's noise floor. Table 5.1 lists the flicker noise coefficients for the devices tested.

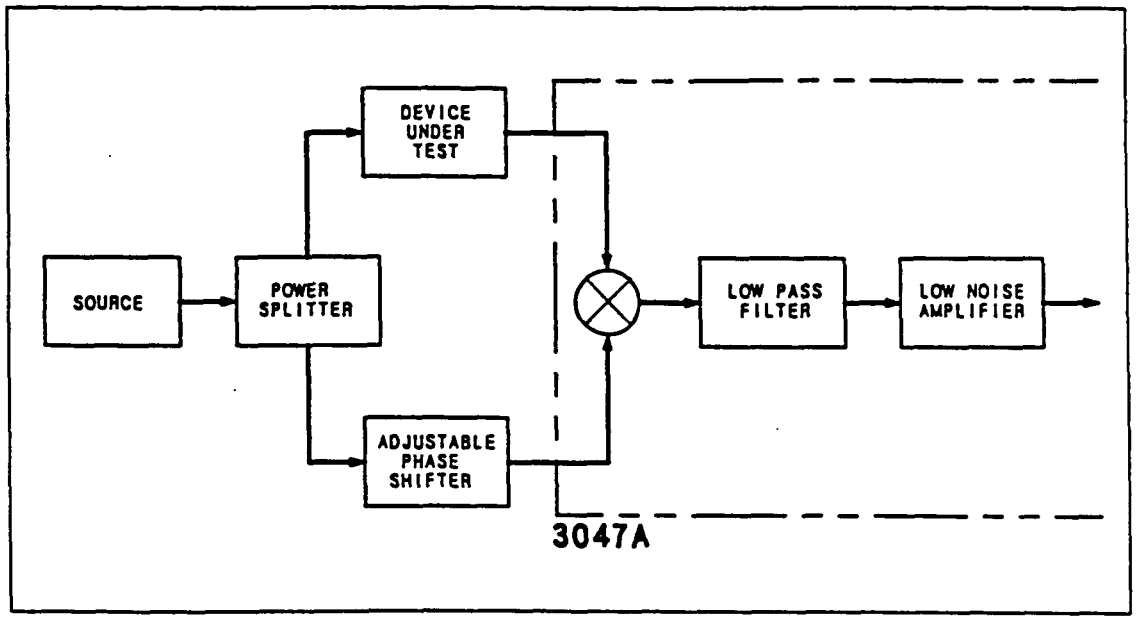
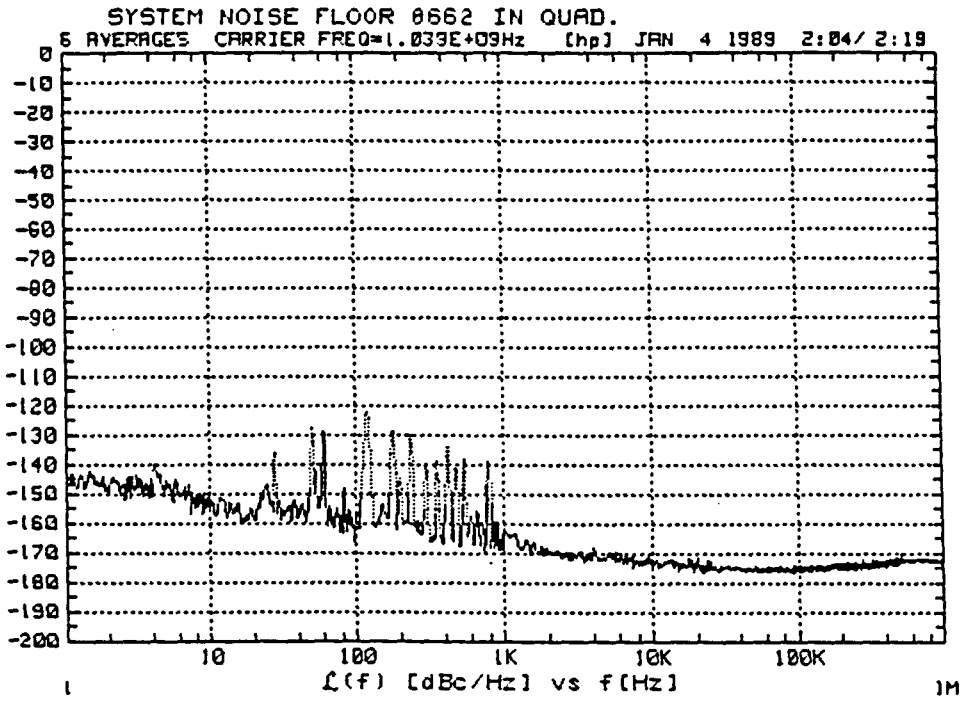


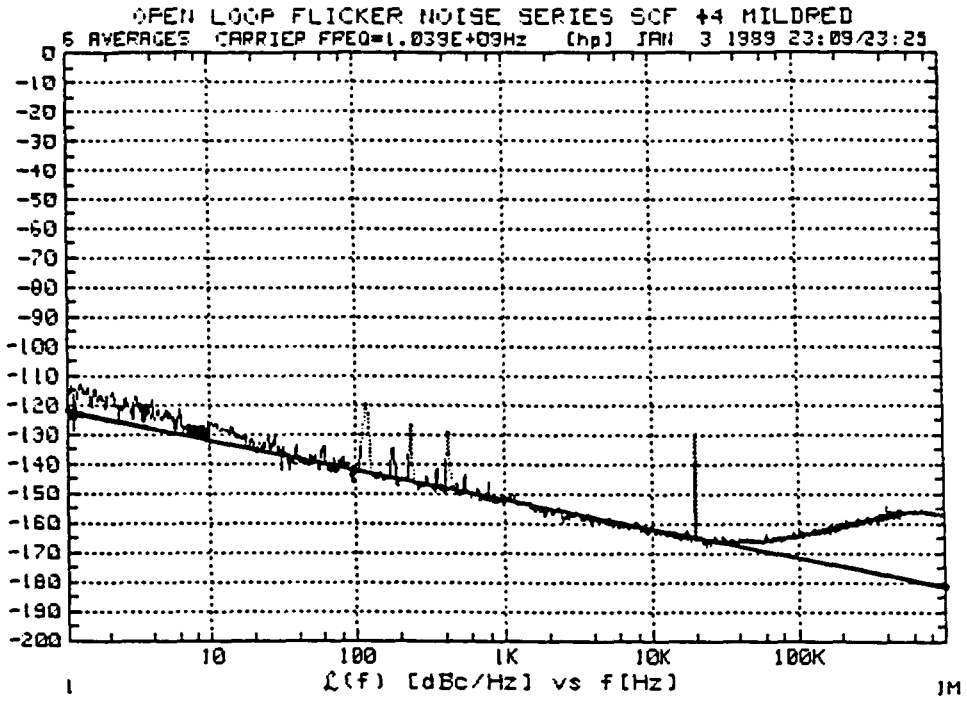
Fig. 5.2
Open Loop Flicker Noise Measurement Setup



PRESENT SOURCE CHARACTERISTICS
CENTER VOLTAGE OF TUNING CURVE= 0 Volts
VOLTAGE TUNING RANGE=+- 9.99 Volts
TOTAL FREQUENCY TUNING RANGE IS <=1 MHz
PHASE DETECTOR INPUT FREQ=1.03900E+09 Hz
CARRIER FREQ=1.03900E+09 Hz
INTERNAL MIXER IS 0, (5MHz-1.6 GHz)

PRESENT MEASUREMENT CONST ANTS
VCOSLOPE= 0 Hz/V
LOW NOISE AMPLIFIER IS IN
ACCURACY SPEC DEGRADATION= 0 dB
PHASESLOPE= .33 VOLTS DC OFFSET OF MIXER= 0 VOLTS
LOOPBW1= 0 Hz LOOPBW3= 0 Hz
ZERO FREQ IN LAG-LEAD= 1.59154943092E+9 Hz
ATTEN1 = 1 ATTEN2 = 1

Fig. 5.3
HP3047 System Noise Floor



PRESENT SOURCE CHARACTERISTICS
CENTER VOLTAGE OF TUNING CURVE= 0 Volts
VOLTAGE TUNING RANGE=+- 9.99 Volts
TOTAL FREQUENCY TUNING RANGE IS <=1 MHz
PHASE DETECTOR INPUT FREQ=1.03920E+09 Hz
CARRIER FREQ=1.03920E+09 Hz
INTERNAL MIXER IS 0, (5MHz-1.6 GHz)
PRESENT MEASUREMENT CONSTANTS
VCOSLOPE= 0 Hz/V
LOW NOISE AMPLIFIER IS IN
ACCURACY SPEC DEGRADATION= 0 dB
PHASESLOPE= .2 VOLTS DC OFFSET OF MIXER= 0 VOLTS
LOOPBW1= 0 Hz LOOPBW3= 0 Hz
ZERO FREQ IN LAG-LEAD= 1.59154943092E+9 Hz
ATTEN1 = 1 ATTEN2 = 1

Fig. 5.4
Typical SCF Flicker Noise Measurement

Table 5.1 Open Loop Flicker Noise Measurements

Device Under Test	L(f) at 1 Hz (dBc/Hz)	α (sec^{-1})
SCF #1	-128	1.6×10^{-13}
SCF #2 (VCO)	-118	1.6×10^{-12}
SCF #3	-119	1.3×10^{-12}
SCF #4 (Simple Osc.)	-122	6.3×10^{-13}
SCF #5 (OMSCF + SCF)	-115	3.2×10^{-12}
Varactor #1	-130	1.0×10^{-13}
MAR 6 (0 dB Comp.)	-120	1.0×10^{-12}
(1 dB Comp.)	-122	6.3×10^{-13}
(3 dB Comp.)	-120	1.0×10^{-12}
(5 dB Comp.)	-122	6.3×10^{-13}
(7 dB Comp.)	-125	3.2×10^{-13}
11729 LNA (20 dB Comp.)	-122	6.3×10^{-13}
MAR 7 (0 dB Comp.)	-122	6.3×10^{-13}
(1 dB Comp.)	-123	5.0×10^{-13}
(3 dB Comp.)	-120	1.0×10^{-12}
(5 dB Comp.)	-123	5.0×10^{-13}
(7 dB Comp.)	-124	4.0×10^{-13}

This was determined by extrapolating the 1/f slope to 1 Hz. and calculating α using Eq. 5.5.

$$\alpha = \text{Log}^{-1}[L(f)/10]\big|_{fm = 1\ Hz} \tag{5.5}$$

The values shown for the filters range over an order of magnitude from 1.6×10^{-13} to 3.2×10^{-12} sec^{-1}, which is typical for flicker noise measurements of otherwise similar devices as mentioned above. The amplifiers were observed under various degrees of compression in order to see the effect, if any, on the flicker noise. Attenuating pads were used at the inputs to the amplifiers in order to vary the drive level to the amplifiers. This caused some concern, since additional padding tends to bury the signal into the noise before it reaches the amplifier. For small values of attenuation, the pads do not create a serious problem, but measurements on two types of 20 dB attenuators seem to indicate that their inclusion dominates the measurement. The measurements listed for the amplifiers may be considered to be pessimistic. Tests on silicon bipolar amplifiers conducted by Parker resulted in measurements ranging from -140 to -125 dBc/Hz at 1 Hz, with -135 dBc/Hz at 1 Hz, or 3.2×10^{-14} sec^{-1} being typical [19]. In this case, the filters may be considered to have a dominant effect on the flicker noise performance of the oscillators. If, on the other hand, the measurements are a true reflection of the amplifier's performance, then the amplifiers and filters are more likely to contribute approximately equally to the measured flicker noise. In any case, a dependence on compression level was not observed.

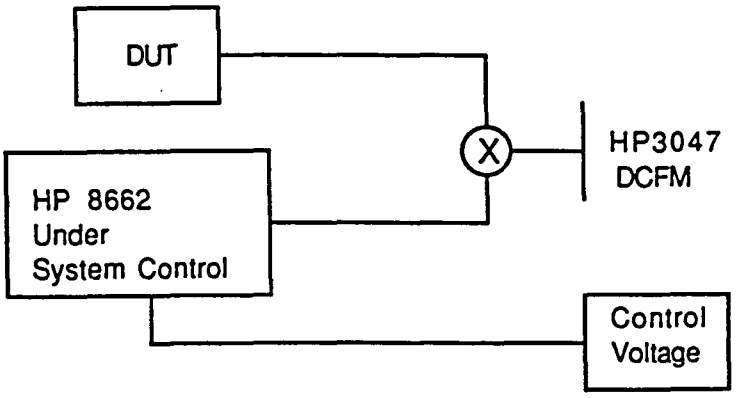


Fig. 5.5
Closed Loop DCFM Phase Noise Measurement Setup

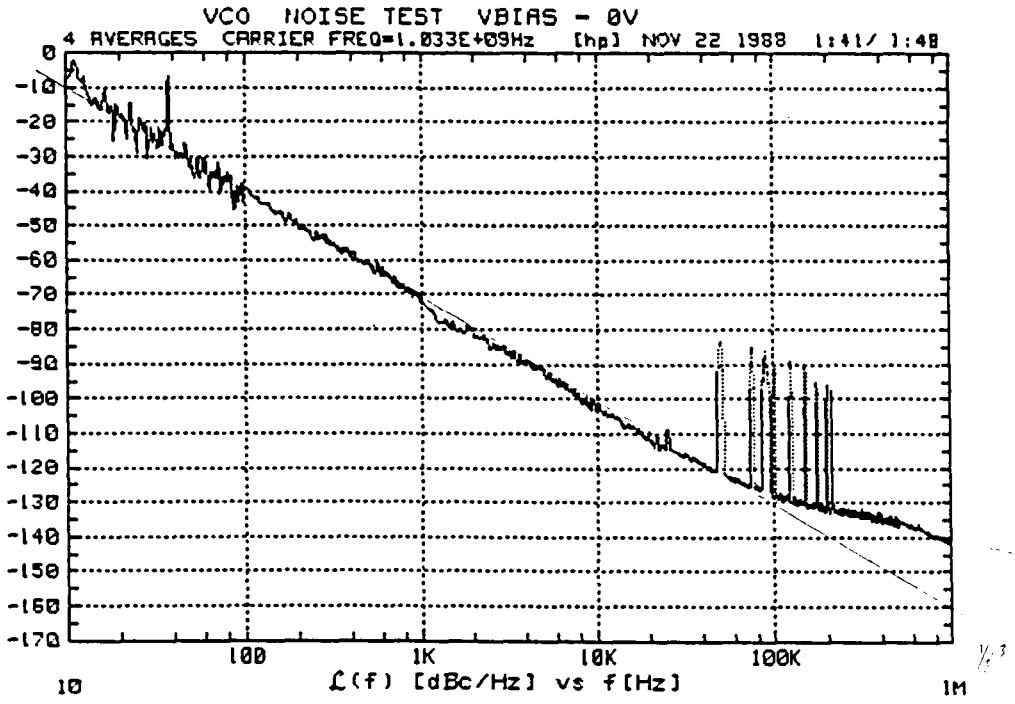
5.3. Oscillator Phase Noise Measurements

The HP 3047 Phase Noise Measurement System is designed to analyze the phase noise of very stable sources and has the added feature that discriminates between random noise sources which are normalized to a 1 Hz bandwidth and deterministic signals such as power line frequencies which show up as spurs on the phase noise plot [21]. The most suitable method of measuring phase noise of an oscillator involves phase locking a source with superior phase noise performance to the source under test, mixing the signals down to base band and measuring the noise power at frequency offsets using low frequency spectrum analyzers with superior dynamic range and noise floors in comparison with those at higher frequencies. A block diagram of the measurement set up is shown in Fig. 5.5. The HP3047 offers two options for making voltage controlled phase noise measurements: dc frequency modulation (DCFM) which is a wide band voltage control method, and electronic frequency control (EFC) which has a very small tuning range and lower noise floor which is used to analyze very stable sources. DCFM was the method of choice since it allowed the system to track the frequency drift of the free running oscillator without losing lock.

Various methods of measuring the phase noise of the VCO at a fixed frequency (varactor bias = 0 V) of 1.0328 GHz are presented in Figs. 5.6a through e. The first of these involved attenuating the output to be less than the maximum input level of the buffer amp.

In this case, a Mini Circuits amplifier was used providing 13 dB of gain and -18 dB of return loss. The next technique was similar but involved using the LNA of the HP11729 Carrier Noise Test Set and splitting the power so that the signal could be monitored on the spectrum analyzer. A third method employed a circulator to provide a sample of the output to the system. The return loss is low, and no additional noise is introduced due to attenuation and amplification. In Fig. 5.6d a dual directional coupler was used to provide a signal from its 20 dB port. Amplification was necessary ahead of the coupler to provide an adequate signal level although in this case, with no attenuation ahead of the amplifier, it was operating in a saturated condition. Finally, an Avantek amplifier was used to amplify the signal out of the directional coupler and was seen to slightly degrade the measurement. This was most likely due to the noisiness of the amplifier. Methods a - d indicate a $1/f^3$ slope for the TFR based VCO with consistent values of -70 dBc/Hz at 1 kHz.

In the block diagram of Fig. 5.5, the roles of the HP8662 and the TFR based VCO were interchanged with the HP8662 operating at a fixed frequency and the VCO being controlled by the system. The VCO slope and tuning center voltage were entered into the system which automatically determines the closed loop PLL parameters. The plot shown in Fig. 5.7 is identical to those shown in Figs. 5.2a through d. What this represents is not the phase noise of the HP8662, but rather the noise floor of the measurement system which has been degraded by the TFR based VCO and is thus indicative of its phase noise performance.



PRESENT SOURCE CHARACTERISTICS
CENTER VOLTAGE OF TUNING CURVE= 0 Volts
VOLTAGE TUNING RANGE=+- 9.99 Volts
TOTAL FREQUENCY TUNING RANGE= 3.996E+6
PHASE DETECTOR INPUT FREQ=1.03285E+09 Hz
CARRIER FREQ=1.03270E+09 Hz
INTERNAL MIXER IS 0, (5MHz-1.6 GHz)

PRESENT MEASUREMENT CONST ANTS
VCOSLOPE= 190476.19 Hz/V
LOW NOISE AMPLIFIER IS IN
ACCURACY SPEC DEGRADATION= 1.06 dB
PHASESLOPE= .063 VOLTS DC OFFSET OF MIXER=-.0049 VOLTS
LOOPBW1= 1.136654893E+6 Hz LOOPBW3= 7219.51 Hz
ZERO FREQ IN LAG-LEAD= 1985 Hz
ATTEN1 = 1 ATTEN2 = 1

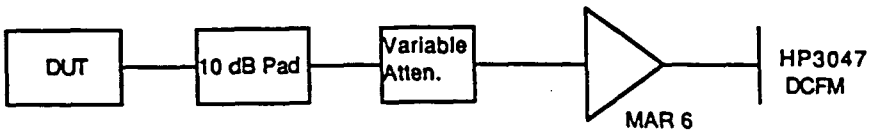
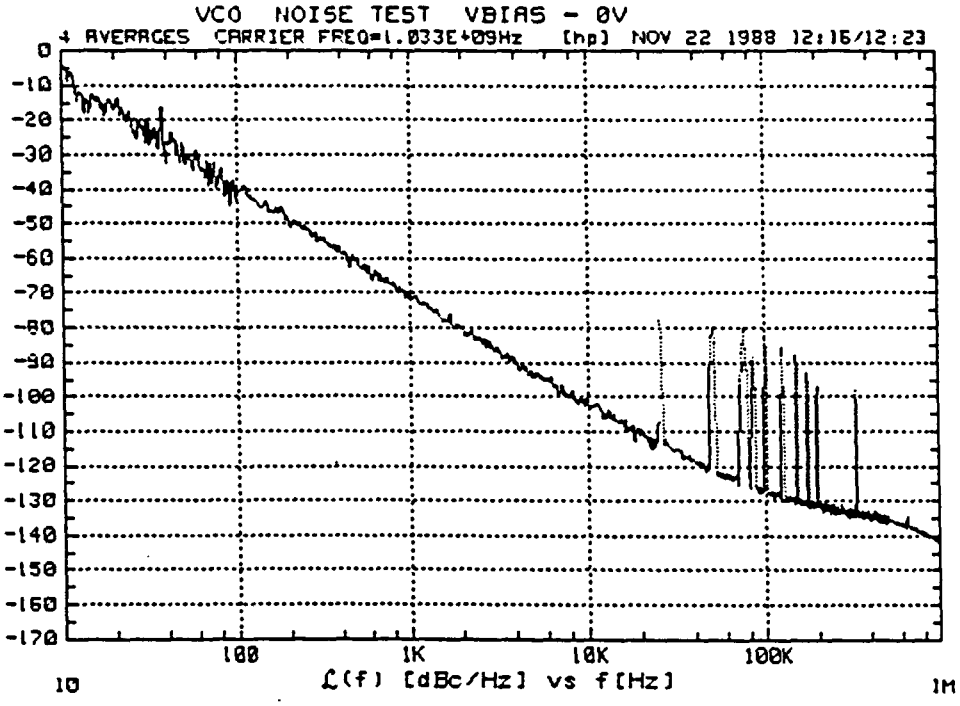


Fig. 5.6a
Phase Noise Method Using Buffer Amp



PRESENT SOURCE CHARACTERISTICS
CENTER VOLTAGE OF TUNING CURVE= 0 Volts
VOLTAGE TUNING RANGE=+- 9.99 Volts
TOTAL FREQUENCY TUNING RANGE= 3.996E+6
PHASE DETECTOR INPUT FREQ=1.03277E+09 Hz
CARRIER FREQ=1.03270E+09 Hz
INTERNAL MIXER IS 0, (5MHz-1.6 GHz)

PRESENT MEASUREMENT CONST ANTS
VCOSLOPE= 190476.19 Hz/V
LOW NOISE AMPLIFIER IS IN
ACCURACY SPEC DEGRADATION= 0 dB
PHASESLOPE= .37 VOLTS DC OFFSET OF MIXER= .0033 VOLTS
LOOPBW1= 1.38150553056E+6 Hz LOOPBW3= 6720 Hz
ZERO FREQ IN LAG-LEAD= 1985 Hz
ATTEN1 = 1 ATTEN2 = 1

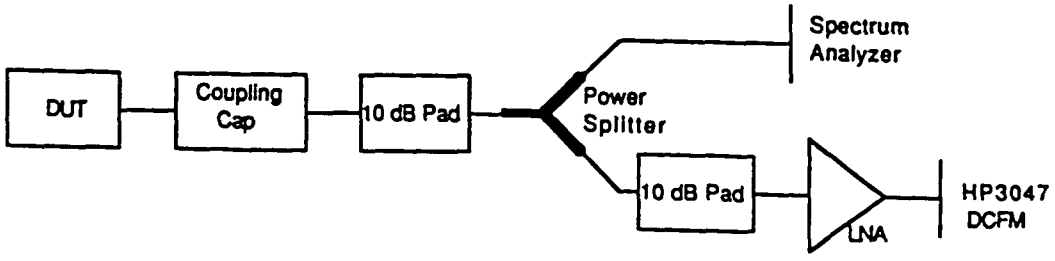
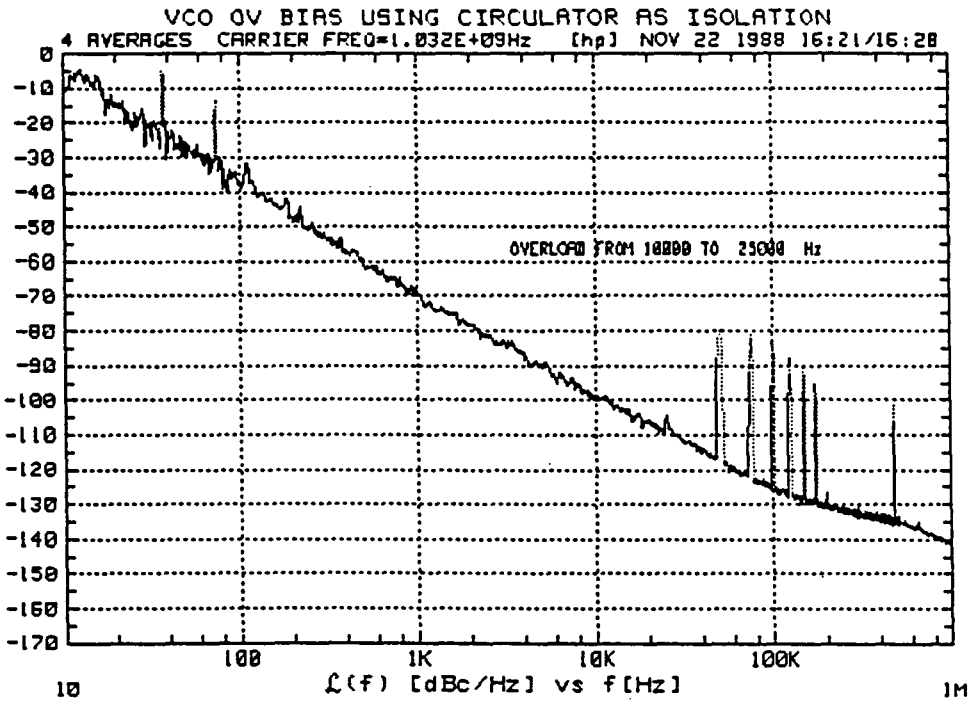


Fig. 5.6b
Phase Noise Method Using LNA



PRESENT SOURCE CHARACTERISTICS
CENTER VOLTAGE OF TUNING CURVE= 0 Volts
VOLTAGE TUNING RANGE=+- 9.99 Volts
TOTAL FREQUENCY TUNING RANGE= 3.996E+6
PHASE DETECTOR INPUT FREQ=1.03163E+09 Hz
CARRIER FREQ=1.03160E+09 Hz
INTERNAL MIXER IS 0, (5MHz-1.6 GHz)

PRESENT MEASUREMENT CONST ANTS
VCOSLOPE= 190476.19 Hz/V
LOW NOISE AMPLIFIER IS IN
ACCURACY SPEC DEGRADATION= 0 dB
PHASESLOPE= .022 VOLTS DC OFFSET OF MIXER=-.0005 VOLTS
LOOPBW1= 1.46218545063E+6 Hz LOOPBW3= 7979.18 Hz
ZERO FREQ IN LAG-LEAD= 1985 Hz
ATTEN1 = 1 ATTEN2 = 1

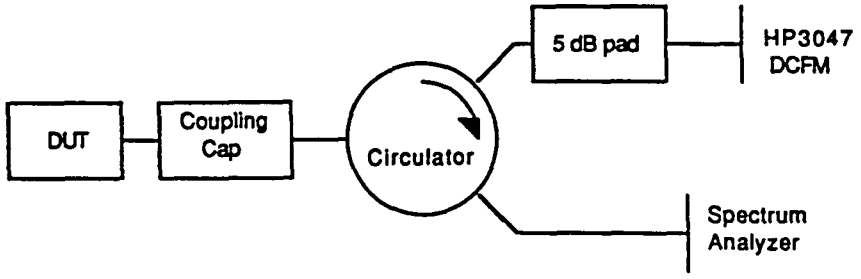
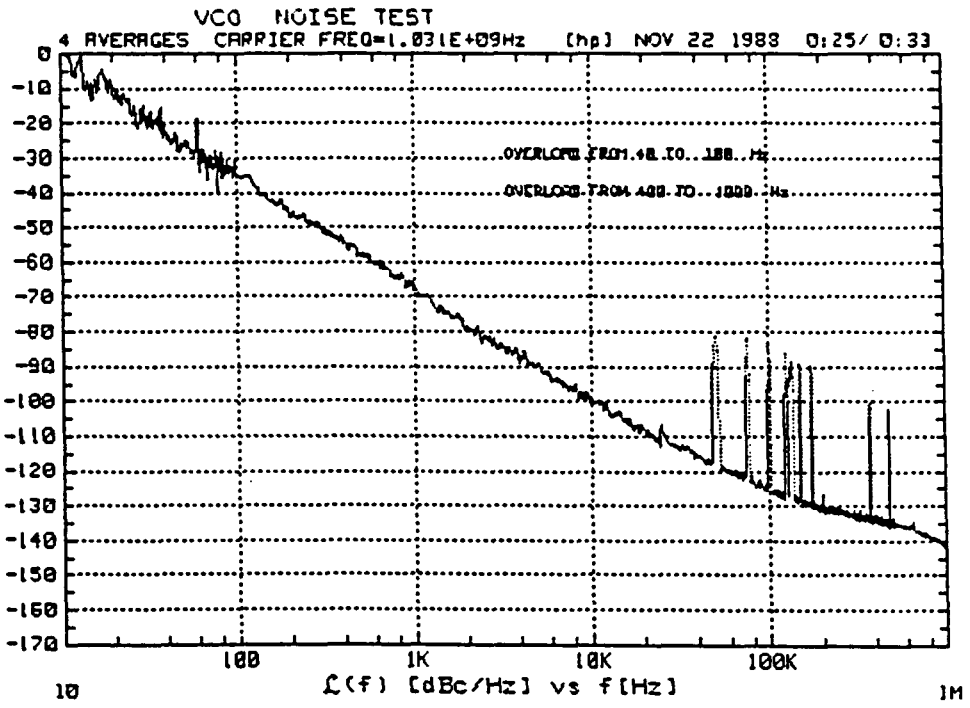


Fig. 5.6c
Phase Noise Method Using Circulator



PRESENT SOURCE CHARACTERISTICS
CENTER VOLTAGE OF TUNING CURVE= 0 Volts
VOLTAGE TUNING RANGE=+- 9.99 Volts
TOTAL FREQUENCY TUNING RANGE= 3.996E+6
PHASE DETECTOR INPUT FREQ=1.03126E+09 Hz
CARRIER FREQ=1.03140E+09 Hz
INTERNAL MIXER IS 0, (5MHz-1.6 GHz)

PRESENT MEASUREMENT CONST ANTS
VCOSLOPE= 190476.19 Hz/V
LOW NOISE AMPLIFIER IS IN
ACCURACY SPEC DEGRADATION= 0 dB
PHASESLOPE= .054 VOLTS DC OFFSET OF MIXER= .0005 VOLTS
LOOPBW1= 1.39969625304E+6 Hz LOOPBW3= 7790.42 Hz
ZERO FREQ IN LAG-LEAD= 1985 Hz
ATTEN1 = 1 ATTEN2 = 1

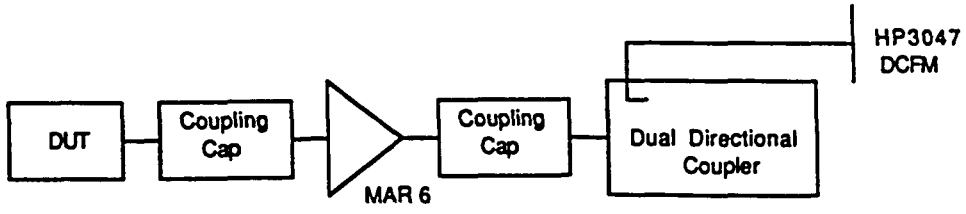
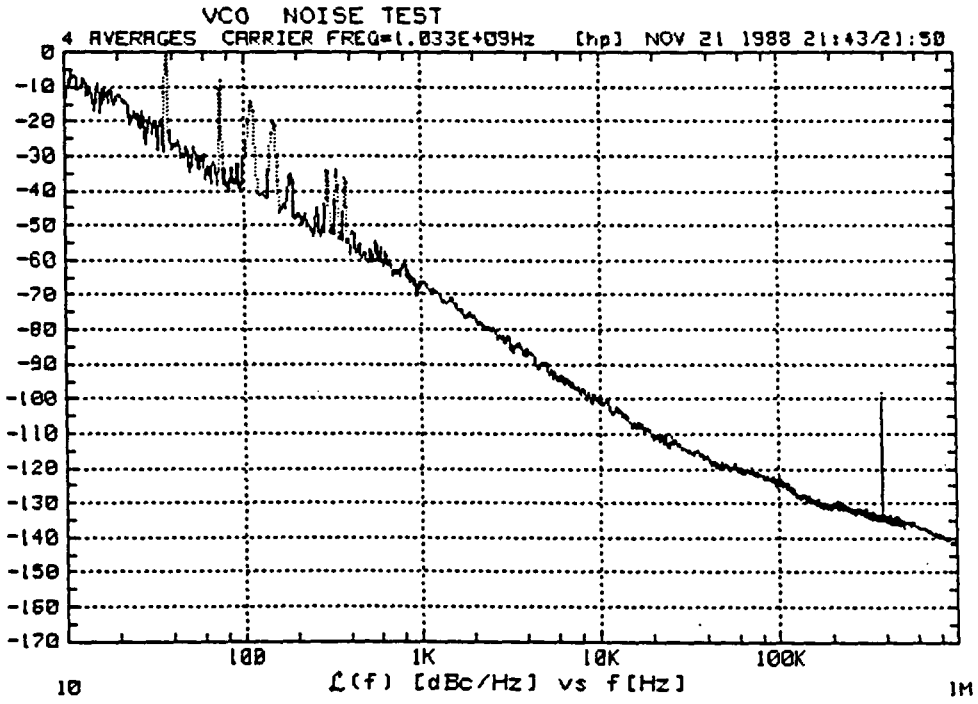


Fig. 5.6d
Phase Noise Method Using Directional Coupler



PRESENT SOURCE CHARACTERISTICS
CENTER VOLTAGE OF TUNING CURVE= 0 Volts
VOLTAGE TUNING RANGE=+- 9.99 Volts
TOTAL FREQUENCY TUNING RANGE= 3.996E+6
PHASE DETECTOR INPUT FREQ=1.03274E+09 Hz
CARRIER FREQ=1.03280E+09 Hz
INTERNAL MIXER IS 0, (5MHz-1.6 GHz)

PRESENT MEASUREMENT CONSTANTS
VCOSLOPE= 190476.19 Hz/V
LOW NOISE AMPLIFIER IS IN
ACCURACY SPEC DEGRADATION= 0 dB
PHASESLOPE= .268 VOLTS DC OFFSET OF MIXER= .009 VOLTS
LOOPBW1= 1.5454255468E+6 Hz LOOPBW3= 7714.4 Hz
ZERO FREQ IN LAG-LEAD= 1985 Hz
ATTEN1 = 1 ATTEN2 = 1

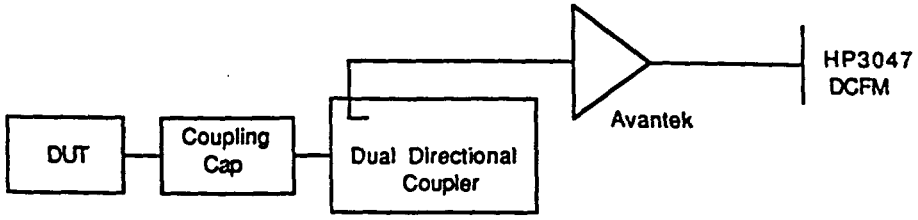
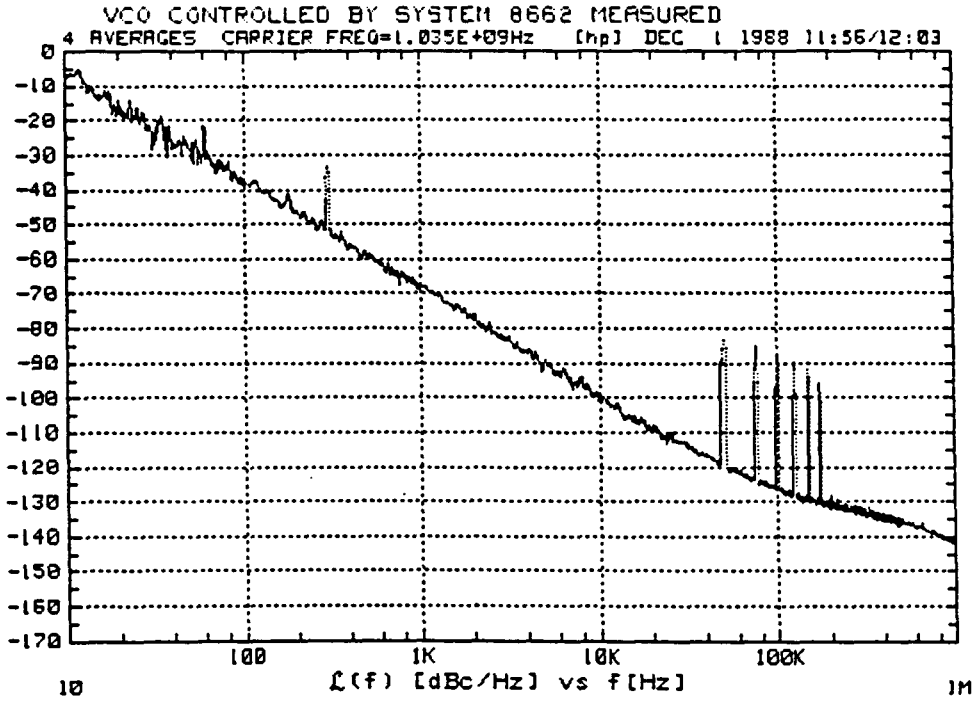


Fig. 5.6e
Unacceptable Phase Noise Method



PRESENT SOURCE CHARACTERISTICS
CENTER VOLTAGE OF TUNING CURVE= 6.975 Volts
VOLTAGE TUNING RANGE=+- 1.98 Volts
TOTAL FREQUENCY TUNING RANGE= 2.E+6
PHASE DETECTOR INPUT FREQ=1.03500E+09 Hz
CARRIER FREQ=1.03500E+09 Hz
INTERNAL MIXER IS 0, (5MHz-1.6 GHz)
PRESENT MEASUREMENT CONST ANTS
VCOSLOPE= 665113.116 Hz/V
LOW NOISE AMPLIFIER IS IN
ACCURACY SPEC DEGRADATION= 0 dB
PHASESLOPE= .376 VOLTS DC OFFSET OF MIXER= .0093 VOLTS
LOOPBW1= 994692.947607 Hz LOOPBW3= 4757.06 Hz
ZERO FREQ IN LAG-LEAD= 1985 Hz
ATTEN1 = 1 ATTEN2 = .5

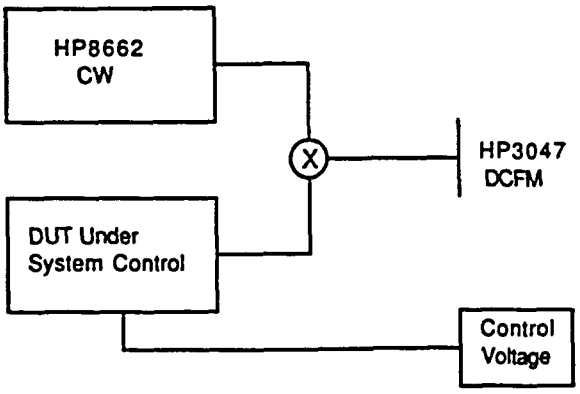


Fig. 5.7
TFR Based VCO Under System Voltage Control

As a further means of verification, tests were conducted at the Avionics Laboratory at Rockwell Collins in Cedar Rapids where an HP3048 phase noise measurement system (an upgrade on the HP3047) was employed. In order to verify that the system noise floor of the HP3048 using DCFM was indeed below the measured performance of the TFR based oscillators, a low noise reference, an HP8642 signal generator, was tested in place of the TFR based oscillators. Its measured phase noise is plotted in Fig. 5.8a and compares favorably to the specified performance shown in Fig. 5.8b. It is seen that the noise floor of the HP8642 is well below that of the TFR based VCO and thus, we can use the DCFM method with a high degree of confidence. Figs. 5.9a and b are plots of the phase noise of the TFR based VCO as measured on the HP3048 with the VCO used as the DUT and under system voltage control respectively. The results agree with the HP3047 measurements within a few dB and exhibit the same characteristic $1/f^3$ slope.

The noise performance of the VCO is essentially the same as that of a simple oscillator using a stacked crystal filter. Plots of two identical simple oscillators are shown in Figs. 5.10a and b. One could conclude then that the phase noise of the SCF based oscillators is dominated by the Q of the filter used in the feedback network and the flicker noise of either the amplifier or filter. For a SCF with a loaded Q of 35 it is likely that the tuning network introduces little degradation to the noise performance.

A final method of measuring phase noise employed the two identical simple oscillators as shown schematically in Fig. 5.11. This particular

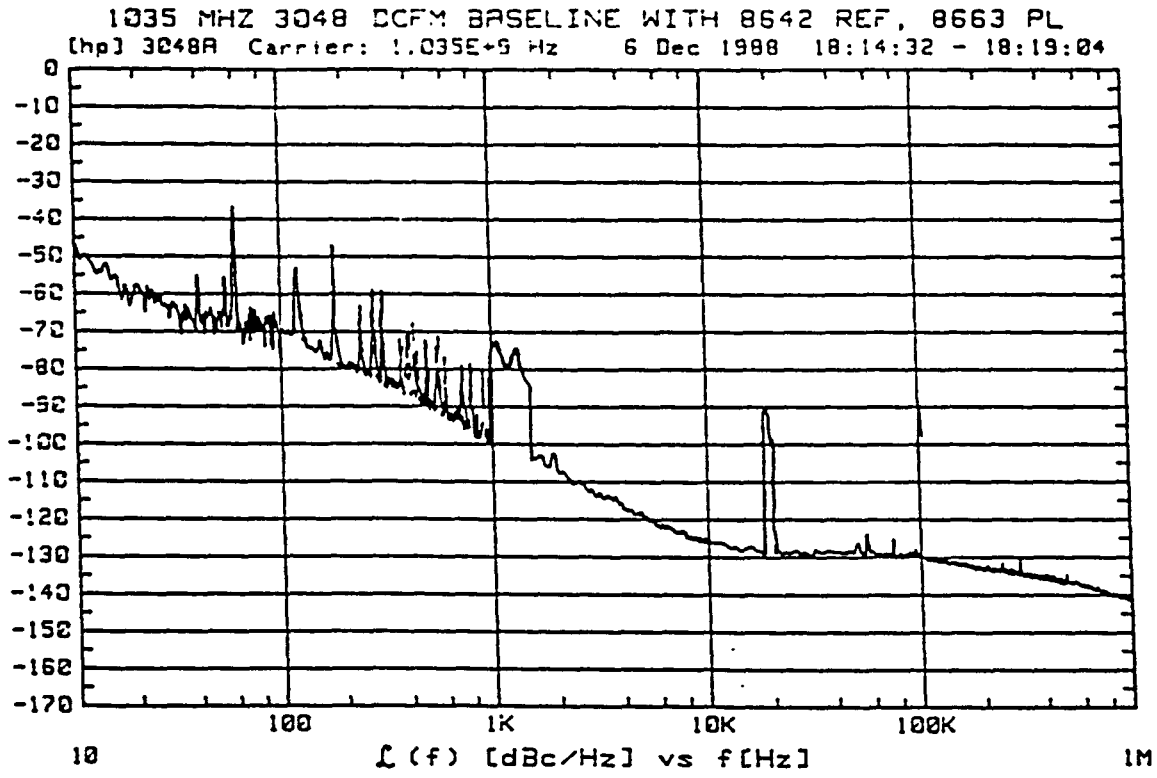


Fig. 5.8a
DCFM Method Applied to Low Noise Source (HP8642)

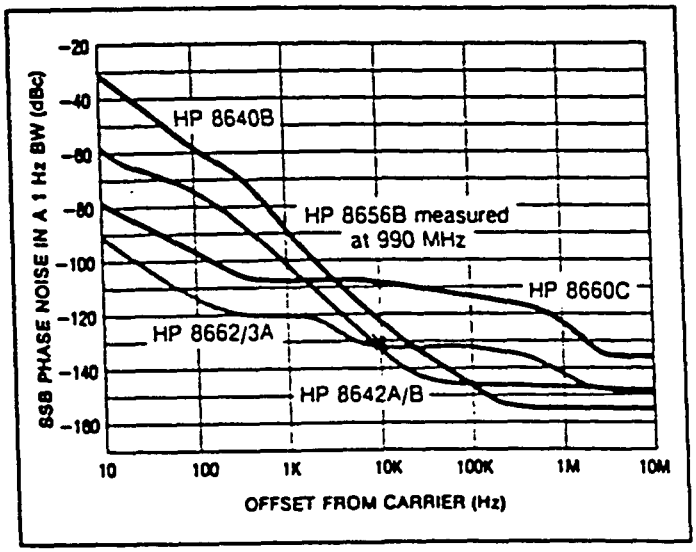


Fig. 5.8b
Specified HP8642 Noise Performance

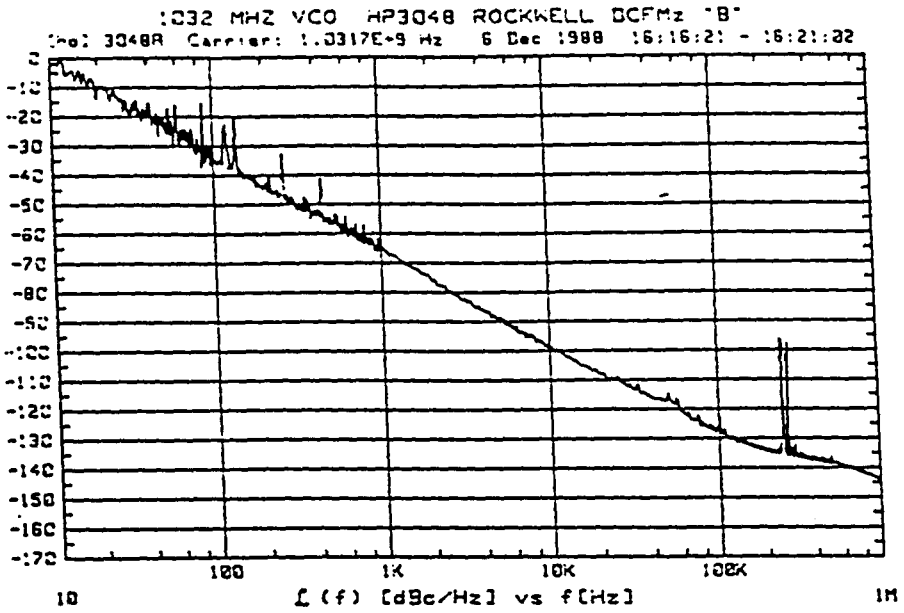


Fig. 5.9a
HP3048 DCFM Measurement of VCO

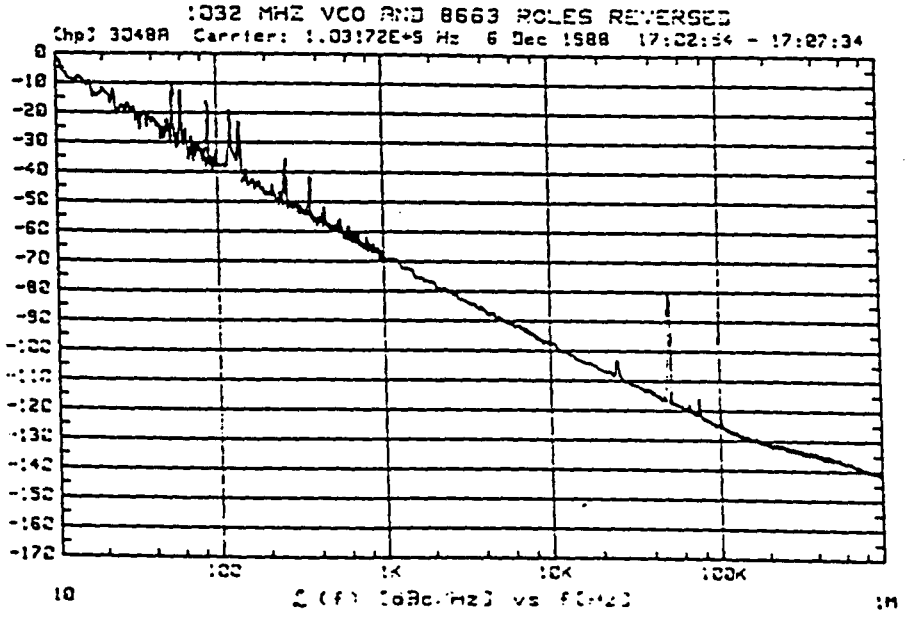
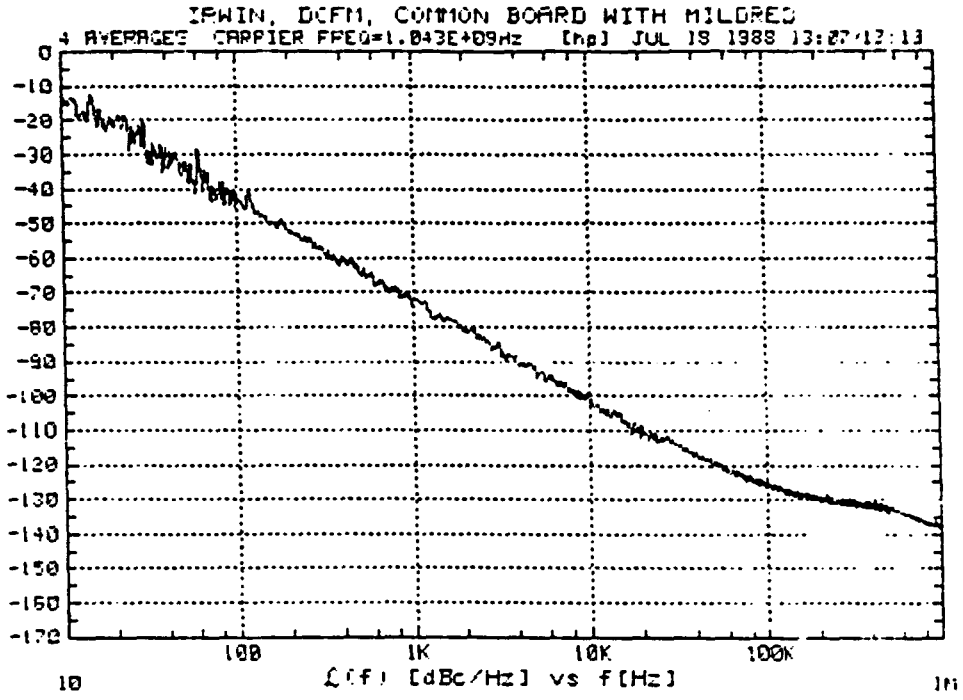


Fig. 5.9b
TFR Based VCO Under HP3048 System Voltage Control



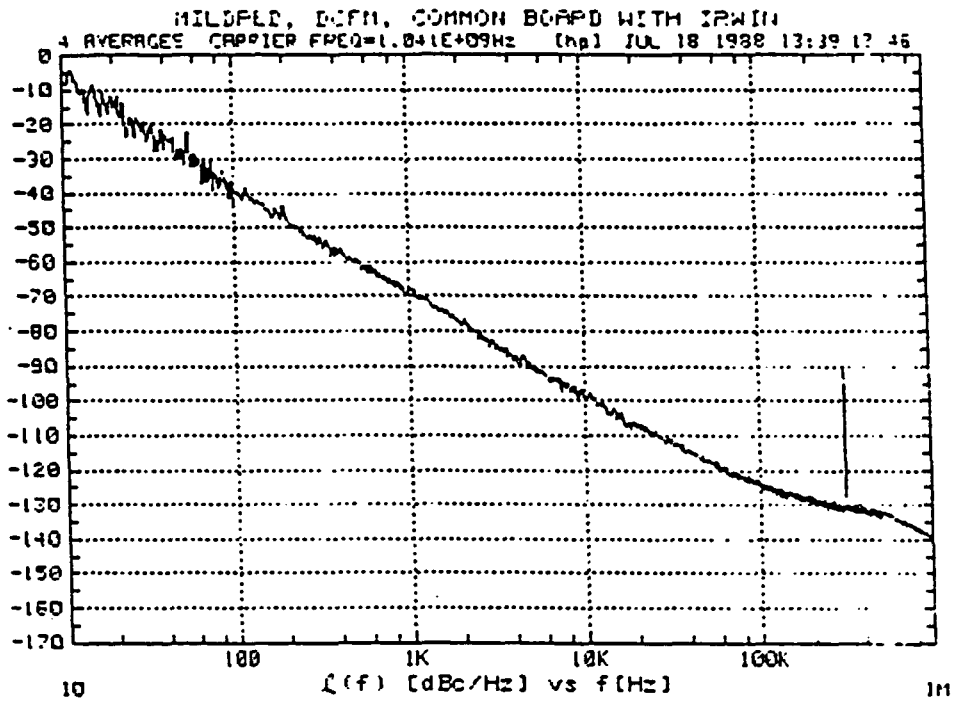
PRESENT SOURCE CHARACTERISTICS

CENTER VOLTAGE OF TUNING CURVE= 0 Volts
VOLTAGE TUNING RANGE=+- 9.99 Volts
TOTAL FREQUENCY TUNING RANGE= 3.996E+6
PHASE DETECTOR INPUT FREQ=1.04202E+09 Hz
CARRIER FREQ=1.04254E+09 Hz
INTERNAL MIXER IS 0, (5MHz-1.6 GHz)

PRESENT MEASUREMENT CONSTANTS

VCOSLOPE= 190476.19 Hz/V
LOW NOISE AMPLIFIER IS IN
ACCURACY SPEC DEGRADATION= 0 dB
PHASESLOPE= .192 VOLTS DC OFFSET OF MIXER= .0043 VOLTS
LOOPBW1= 1.87157363366E+6 Hz LOOPBW3= 3751.93 Hz
ZERO FREQ IN LAG-LEAD= 1985 Hz
ATTEN1 1 ATTEN2 = 1

Fig. 5.10a
Phase Noise of Simple Oscillator #1



PRESENT SOURCE CHARACTERISTICS
CENTER VOLTAGE OF TUNING CURVE= 0 Volts
VOLTAGE TUNING RANGE=+- 9.99 Volts
TOTAL FREQUENCY TUNING RANGE= 3.996E+6
PHASE DETECTOR INPUT FREQ=1.04076E+09 Hz
CARRIER FREQ=1.04060E+09 Hz
INTERNAL MIXER IS 0, (5MHz-1.6 GHz)
PRESENT MEASUREMENT CONSTANTS
VCOSLOPE= 190476.19 Hz/V
LOW NOISE AMPLIFIER IS IN
ACCURACY SPEC DEGRADATION= 0 dB
PHASESLOPE= .281 VOLTS DC OFFSET OF MIXER= .006 VOLTS
LOOPBW1= 1.7207389047?E+6 Hz LOOPBW3= 8081.81 Hz
ZERO FREQ IN LAG-LEAD= 1985 Hz
ATTEN1 = 1 ATTEN2 = 1

Fig. 5.10b
Phase Noise of Simple Oscillator #2

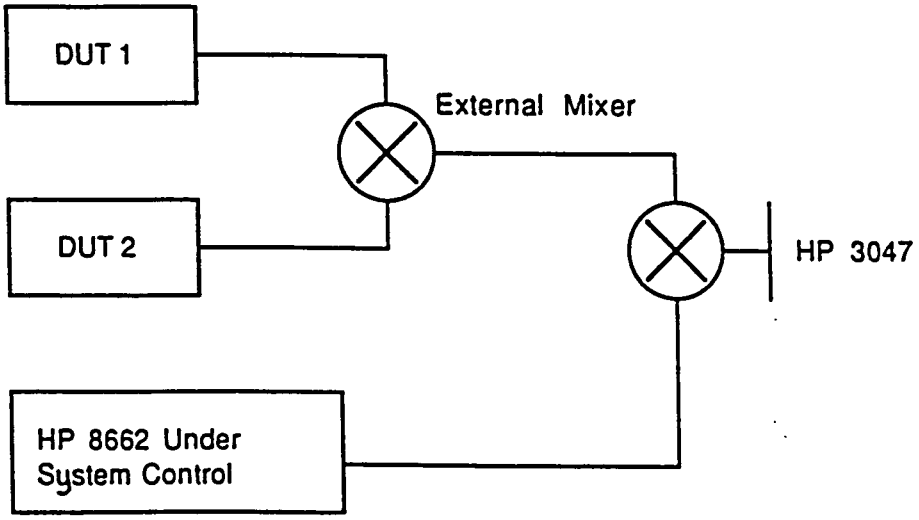
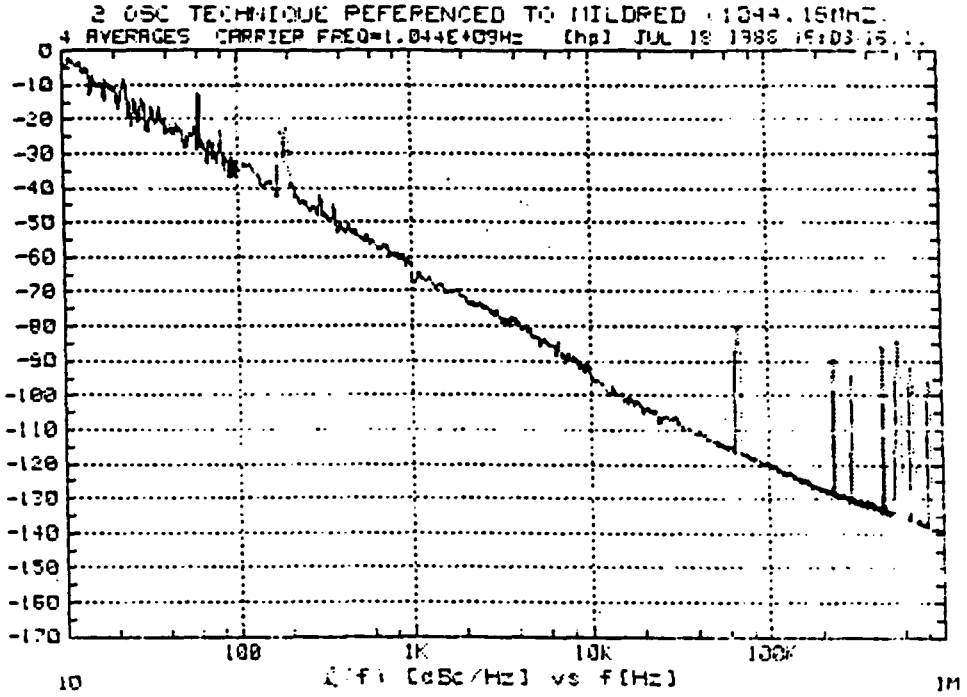
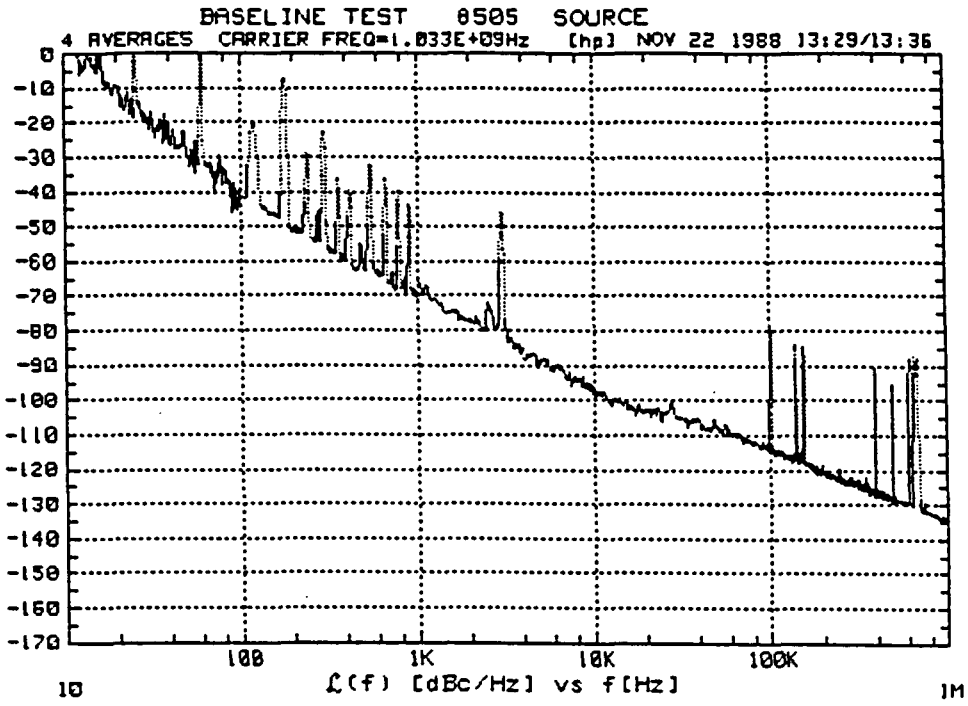


Fig. 5.11
Two Oscillator Measurement Method



PRESENT SOURCE CHARACTERISTICS
CENTER VOLTAGE OF TUNING CURVE= 0 Volts
VOLTAGE TUNING RANGE=+- 9.99 Volts
TOTAL FREQUENCY TUNING RANGE= 1.998E+6
PHASE DETECTOR INPUT FREQ=5.39258E+06 Hz
CARRIER FREQ=1.04415E+09 Hz
INTERNAL MIXER IS 0, (5MHz-1.6 GHz)
PRESENT MEASUREMENT CONST ANTS
VCOSLOPE= 95238.095 Hz/V
LOW NOISE AMPLIFIER IS IN
ACCURACY SPEC DEGRADATION= 0 dB
PHASESLOPE= .36 VOLTS DC OFFSET OF MIXER= .0004 VOLTS
LOOPBW1= 789515.680199 Hz LOOPBW3= 4112.21 Hz
ZERO FREQ IN LAG-LEAD= 1985 Hz
ATTEN1 = 1 ATTEN2 = 1

Fig. 5.12
Phase Noise of Two Oscillators



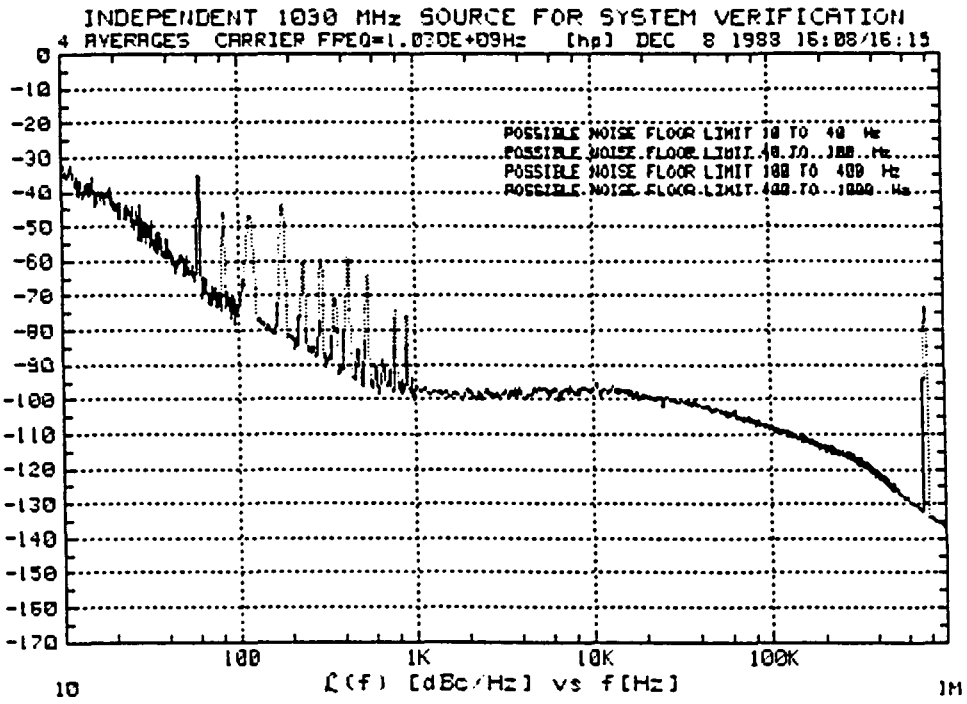
PRESENT SOURCE CHARACTERISTICS

CENTER VOLTAGE OF TUNING CURVE= 0 Volts
VOLTAGE TUNING RANGE=+- 9.99 Volts
TOTAL FREQUENCY TUNING RANGE= 3.996E+6
PHASE DETECTOR INPUT FREQ=1.03285E+09 Hz
CARRIER FREQ=1.03270E+09 Hz
INTERNAL MIXER IS 0, (5MHz-1.6 GHz)

PRESENT MEASUREMENT CONSTANTS

VCOSLOPE= 190476.19 Hz/V
LOW NOISE AMPLIFIER IS IN
ACCURACY SPEC DEGRADATION= 0 dB
PHASESLOPE= .033 VOLTS DC OFFSET OF MIXER= .0005 VOLTS
LOOPBW1= 1.45232712512E+6 Hz LOOPBW3= 7545.38 Hz
ZERO FREQ IN LAG-LEAD= 1985 Hz
ATTEN1 = 1 ATTEN2 = 1

Fig. 5.13
Measured Phase Noise of HP8505 RF Source



PRESENT SOURCE CHARACTERISTICS
CENTER VOLTAGE OF TUNING CURVE= 0 Volts
VOLTAGE TUNING RANGE=+- 9.99 Volts
TOTAL FREQUENCY TUNING RANGE= 3.996E+6
PHASE DETECTOR INPUT FREQ=1.03000E+09 Hz
CARRIER FREQ=1.03000E+09 Hz
INTERNAL MIXER IS 0, (5MHz-1.6 GHz)
PRESENT MEASUREMENT CONSTANTS
VCOSLOPE= 190476.19 Hz/V
LOW NOISE AMPLIFIER IS IN
ACCURACY SPEC DEGRADATION= 0 dB
PHASESLOPE= .323 VOLTS DC OFFSET OF MIXER= .0037 VOLTS
LOOPBW1= 1.49289028398E+6 Hz LOOPBW3= 7384.11 Hz
ZERO FREQ IN LAG-LEAD= 1985 Hz
ATTEN1 = 1 ATTEN2 = 1

Fig. 5.14
Measured Phase Noise of Independent Source

method employs an external mixer which allows one to extract the difference frequency between the two free running oscillators separated by a nominal frequency of 5 MHz, and use the DCFM method to track the difference frequency. The advantage of this method is that the noise is mixed down to a lower frequency before it enters the system so that a lower noise floor and better noise performance of the controlled source are exploited. Fig. 5.12 is a plot of the two oscillators' difference frequency phase noise. Again the $1/f^3$ slope is apparent but the values in dBc/Hz at various offset frequencies are approximately 5 dB higher. One would expect this, since the noise is due to the contribution of both oscillators and should be 3 dB higher than that of a single oscillator. Also, since the oscillators were separated in frequency by 5 MHz, it is quite probable that one or both of the oscillators was operating away from the maximum phase slope which would also degrade the performance.

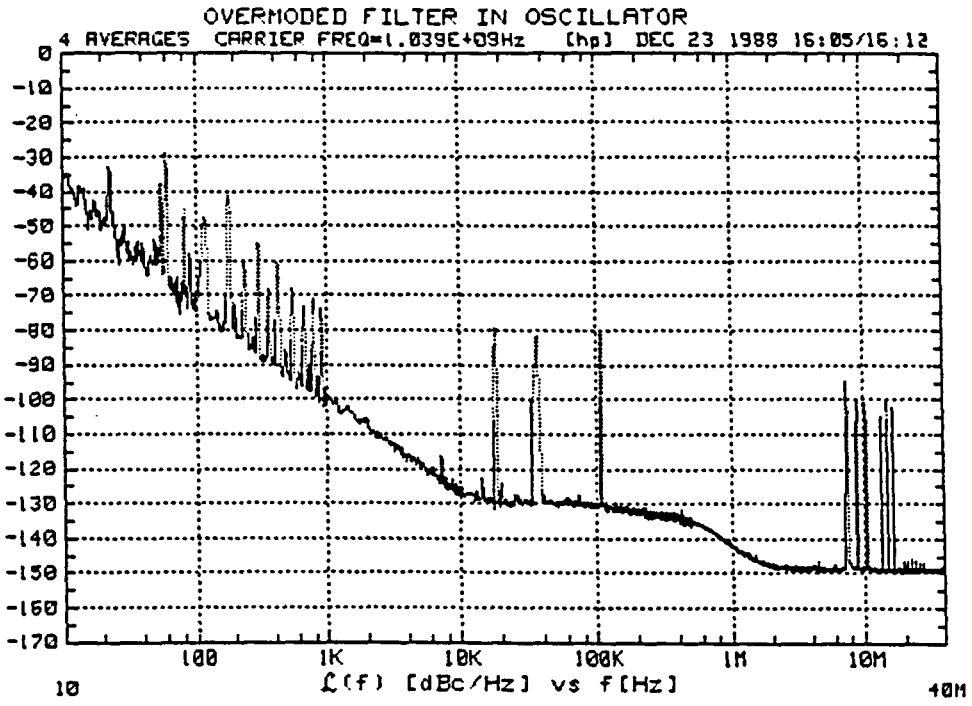
In order to put the phase noise performance of the TFR based oscillators into perspective, a few examples will be provided for comparison. Fig. 5.13 is a phase noise plot of the RF source in an HP8505 network analyzer at a frequency of 1032.8 MHz. It is seen to be of similar quality to the TFR based VCO. Fig. 5.14 is a phase noise plot for a VCO which is phase locked to a more stable reference oscillator. The phase locked VCO exhibits superior performance at lower offset frequencies due to the inherent stability of the reference oscillator. When used in a PLL circuit, the TFR based VCO also exhibited improved phase noise performance. Since the phase noise

system was employed to provide the PLL circuitry, it was not possible to simultaneously make measurements on the system. To observe the improved performance, a HP8566 Spectrum Analyzer was used to measure sideband levels normalized to 1 Hz bandwidths. By referencing the values measured at offset frequencies to the carrier, an equivalent to L(f) was measured. Values of -95.5 dBc/Hz and -98.5 dBc/Hz at offset frequencies of 1 kHz and 6 kHz were measured. These values are much lower than those measured for the free running VCO demonstrating the performance advantage of phase locking to a stable source.

The oscillator based on the overmoded filter structure showed an improvement of 30 dB in phase noise performance in comparison with the simple oscillator and VCO. Initial measurements were made with the oscillator operating at a frequency of 1039.2 MHz. The HP3047 was again used with the DCFM voltage control option selected. A block diagram of the measurement setup and the resulting phase noise plot is shown in Fig. 5.12. Again the $1/f^3$ noise seems to dominate out to the noise floor of the system which occurs at approximately 30kHz. In particular, this circuit achieves a value of -100 dBc/Hz at 1kHz offset from the carrier. In the vicinity of 100 Hz away from the carrier, the slope of the phase noise changes to $1/f^4$ due to random walk effects as discussed in Section 5.1.

5.4. Relating Measured Performance to the Noise Model

In the analysis of Chapter 4, the loaded Q of the filter was determined to be at a maximum somewhere between 1039.15 and 1039.20 MHz. This agrees with the best noise performance measured in this range.



PRESENT SOURCE CHARACTERISTICS
CENTER VOLTAGE OF TUNING CURVE= 0 Volts
VOLTAGE TUNING RANGE=+- 9.99 Volts
TOTAL FREQUENCY TUNING RANGE= 3.996E+6
PHASE DETECTOR INPUT FREQ=1.03920E+09 Hz
CARRIER FREQ=1.03900E+09 Hz
INTERNAL MIXER IS 0, (5MHz-1.6 GHz)

PRESENT MEASUREMENT CONST ANTS
VCOSLOPE= 190476.19 Hz/V
LOW NOISE AMPLIFIER IS IN
ACCURACY SPEC DEGRADATION= 0 dB
PHASESLOPE= .033 VOLTS DC OFFSET OF MIXER= .001 VOLTS
LOOPBW1= 1.52767680795E+6 Hz LOOPBW3= 7548.97 Hz
ZERO FREQ IN LAG-LEAD= 1985 Hz
ATTEN1 = 1 ATTEN2 = 1

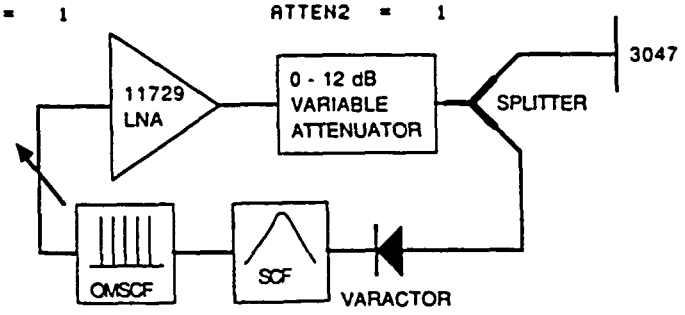
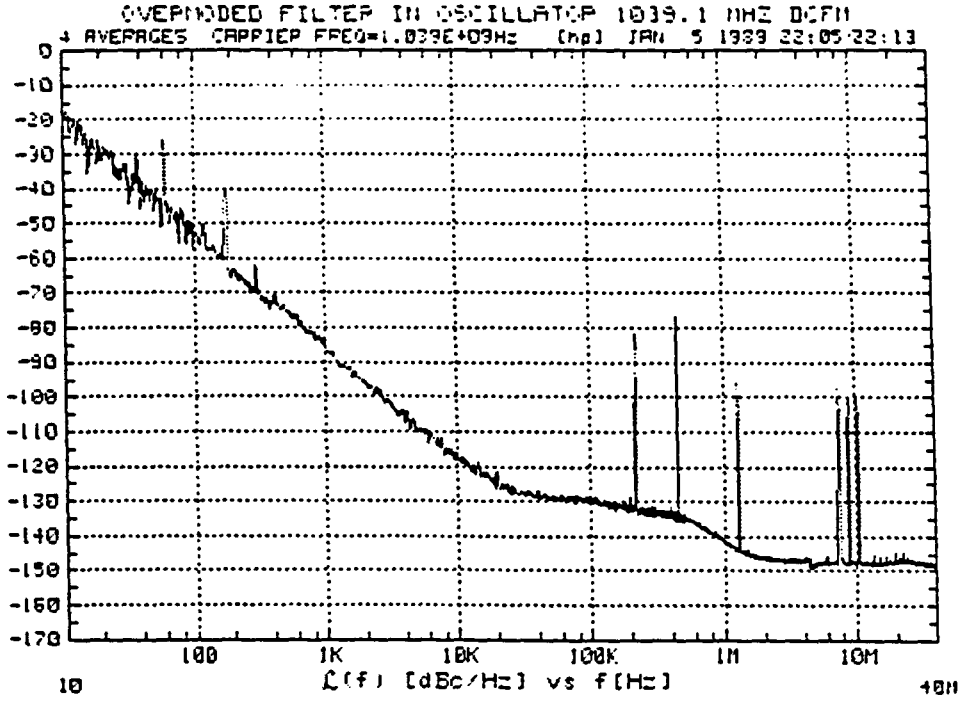


Fig. 5.15
Phase Noise of Selectable Frequency Oscillator

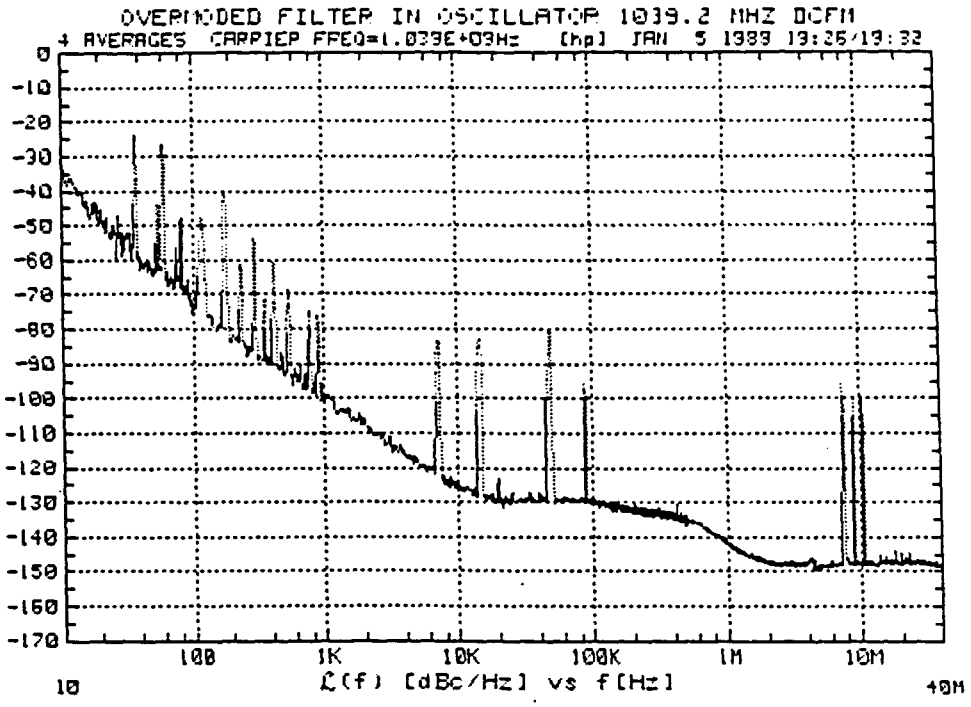


PRESENT SOURCE CHARACTERISTICS
CENTER VOLTAGE OF TUNING CURVE= 0 Volts
VOLTAGE TUNING RANGE=+- 9.99 Volts
TOTAL FREQUENCY TUNING RANGE= 3.996E+6
PHASE DETECTOR INPUT FREQ=1.03912E+09 Hz
CARRIER FREQ=1.03910E+09 Hz
INTERNAL MIXER IS 0, (5MHz-1.6 GHz)
PRESENT MEASUREMENT CONSTANTS
VCOSLOPE= 190476.19 Hz/V
LOW NOISE AMPLIFIER IS IN
ACCURACY SPEC DEGRADATION= 0 dB
PHASESLOPE= .051 VOLTS DC OFFSET OF MIXER= .0026 VOLTS
LOOPBW1= 1.31197597144E+6 Hz LOOPBW3= 7353.78 Hz
ZERO FREQ IN LAG-LEAD= 1985 Hz
ATTEN1 = 1 ATTEN2 = 1

Fig. 5.16
Effect of a Reduction of Q_L on Phase Noise

Fig. 5.16 illustrates the effect of a reduction in the filter's loaded Q as measurements were made at 1039.12 MHz, a few hundred kHz away from the maximum phase slope. A degradation of approximately 15 dB is apparent and may be explained by noting the $1/Q_L^2$ dependence in the first two terms of Eq. 5.4.

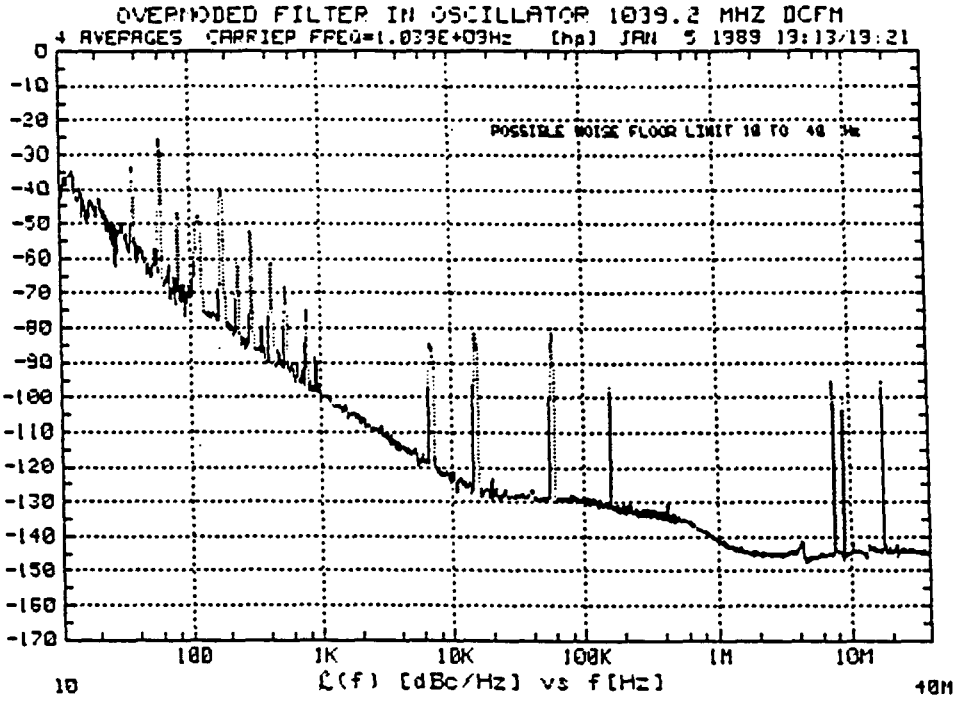
The effect of additional loss in the feedback network was observed and is illustrated in Figs. 5.17a through c. In an attempt to limit the degree of compression in the amplifier, attenuator pads were added in series with the feedback network. Instead of improving performance by limiting gain compression, an increase in attenuation was seen to have an adverse effect on the oscillator's noise at large offset frequencies. This may be explained by noting the last term in Eq. 5.4. As the attenuation in the feedback network is increased, in a closed loop sense, the gain supplied by the amplifier (G) to offset this loss must also increase. In the case where 20 dB of attenuation was introduced, the white noise of the oscillator rose above the noise floor of the measurement system at frequencies outside the bandwidth of the filter. In the vicinity of 10 kHz the presence of a $1/f^2$ slope becomes apparent as the attenuation is increased which is due to thermal effects within the filter's bandwidth multiplied by the higher value of G. At lower offset frequencies, the effect is not as apparent since the flicker noise becomes dominant. Noting this effect provides additional information about the oscillator. It was not possible to measure the bandwidth of the overmoded filter due to frequency resolution



PRESENT SOURCE CHARACTERISTICS
CENTER VOLTAGE OF TUNING CURVE= 0 Volts
VOLTAGE TUNING RANGE=+- 9.99 Volts
TOTAL FREQUENCY TUNING RANGE= 3.996E+6
PHASE DETECTOR INPUT FREQ=1.03918E+09 Hz
CARRIER FREQ=1.03920E+09 Hz
INTERNAL MIXER IS 0, (5MHz-1.6 GHz)

PRESENT MEASUREMENT CONST ANTS
VCOSLOPE= 190476.19 Hz/V
LOW NOISE AMPLIFIER IS IN
ACCURACY SPEC DEGRADATION= 0 dB
PHASESLOPE= .05 VOLTS DC OFFSET OF MIXER= .0034 VOLTS
LOOPBW1= 1.60899268127E+6 Hz LOOPBW3= 8651.5 Hz
ZERO FREQ IN LAG-LEAD= 1985 Hz
ATTEN1 = 1 ATTEN2 = 1

Fig. 5.17a
8 dB of Attenuation Added in Feedback Path



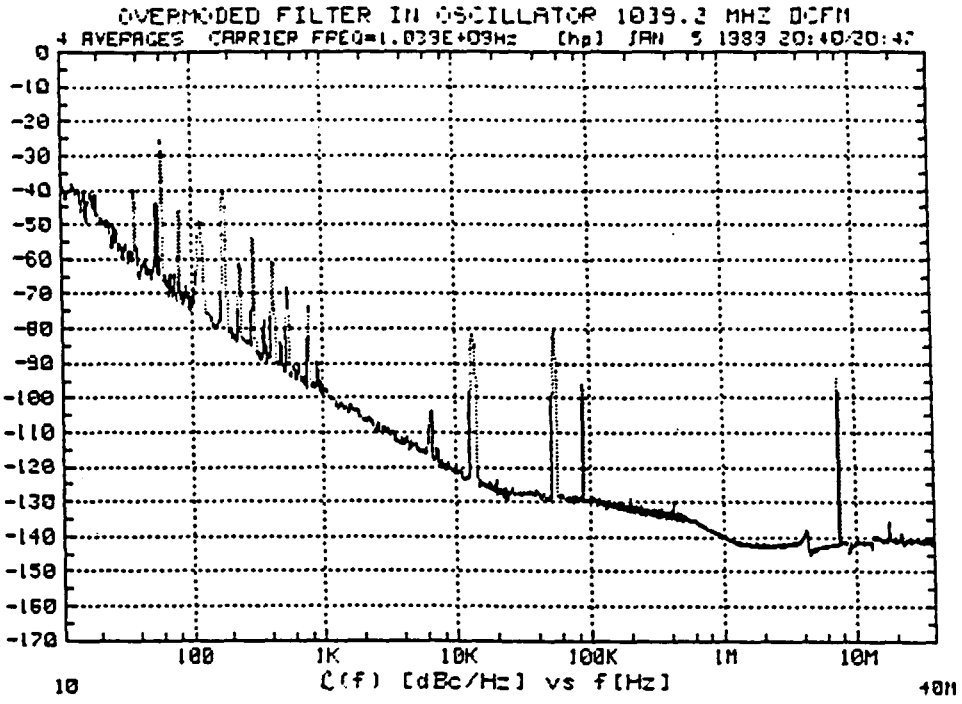
PRESENT SOURCE CHARACTERISTICS

CENTER VOLTAGE OF TUNING CURVE= 0 Volts
VOLTAGE TUNING RANGE=+- 9.99 Volts
TOTAL FREQUENCY TUNING RANGE= 3.996E+6
PHASE DETECTOR INPUT FREQ=1.03917E+09 Hz
CARRIER FREQ=1.03920E+09 Hz
INTERNAL MIXER IS 0, (5MHz-1.6 GHz)

PRESENT MEASUREMENT CONSTANTS

VCOSLOPE= 190476.19 Hz/V
LOW NOISE AMPLIFIER IS IN
ACCURACY SPEC DEGRADATION= 0 dB
PHASESLOPE= .059 VOLTS DC OFFSET OF MIXER= .0033 VOLTS
LOOPBW1= 1.51654559373E+6 Hz LOOPBW3= 8507.31 Hz
ZERO FREQ IN LAG-LEAD= 1985 Hz
ATTEN1 = 1 ATTEN2 = 1

Fig. 5.17b
13 dB of Attenuation Added in Feedback Path



PRESENT SOURCE CHARACTERISTICS

CENTER VOLTAGE OF TUNING CURVE= 0 Volts
VOLTAGE TUNING RANGE=+- 9.99 Volts
TOTAL FREQUENCY TUNING RANGE= 3.996E+6
PHASE DETECTOR INPUT FREQ=1.03918E+09 Hz
CARRIER FREQ=1.03920E+09 Hz
INTERNAL MIXER IS 0, (5MHz-1.6 GHz)

PRESENT MEASUREMENT CONST ANTS

VCOSLOPE= 190476.19 Hz/V
LOW NOISE AMPLIFIER IS IN
ACCURACY SPEC DEGRADATION= 0 dB
PHASESLOPE= .059 VOLTS DC OFFSET OF MIXER= .0033 VOLTS
LOOPBW1= 1.55936014298E+6 Hz LOOPBW3= 8507.31 Hz
ZERO FREQ IN LAG-LEAD= 1985 Hz
ATTEN1 = 1 ATTEN2 = 1

Fig. 5.17c
20dB of Attenuation Added in Feedback Path

limitations on the network analyzer. In addition, the breakpoint where the phase noise slopes change due to noise within the filter's bandwidth, and outside the bandwidth are buried in the system's noise floor. In the case where 20 dB of additional attenuation was added, the oscillator's white noise and $1/f^2$ noise became observable and by drawing asymptotes and noting their intersection, the filter's bandwidth may be estimated to be 150 kHz as shown in Fig. 5.17c.

The $1/f^3$ slope which dominates the performance of the oscillators leads to a closer analysis of Eq. 5.4. The $1/f^3$ noise results from flicker effects within the bandwidth of the filter, and should break into a 1/f slope outside the bandwidth. The 3 dB bandwidth for a series SCF is in the vicinity of 20 MHz. This is near the outer limits of the measurement system, and although a breakpoint may in fact exist, it is most likely buried in the system's noise floor at these frequencies. A value of 1.6×10^{-12} sec^{-1} for α was computed for the filter used in the VCO application. Assuming that the filter's flicker noise played a dominant role, one may compute the expected value of phase noise at various frequencies. From Chapter 4, the loaded Q of the VCO filter was determined to be 35.80. For f_o = 1035 MHz and at an offset frequency of 1 kHz, a value of -72.7 dBc/Hz is computed. If the measured flicker noise of the amplifier is included, a value of -70.6 is obtained. The latter value agrees with the measured response of -70 dB quite well, although the accuracy spec of 4 dB must be kept in mind. The loaded Q of the overmoded filter and SCF combination was determined to be 3025 at 1039.15 MHz. The open loop flicker noise measurements for the series

combination of the SCF and overmoded filter resulted in the determination of $\alpha = 3.2 \times 10^{-12}$ sec^{-1}. Using these values to compute the $1/f^3$ contribution to the phase noise results in a value of -108.3 dBc/Hz at 1 kHz offset. The best measurements obtained at 1039.2 MHz resulted in a value of -100.0 dBc/Hz which agrees with the theory fairly well. It is interesting to note that the oscillators based on the overmoded filter and the SCF exhibited consistent performance, where a significant increase in Q resulted in a significant improvement in noise performance. Also, the flicker noise is seen to play a dominant role in both cases.

5.5. Additional Comments

In measuring the performance of the VCO, many techniques were used to establish a level of confidence in the system. In particular it was important to determine that the noise floor of the system was well below the performance of the DUT. Fig. 5.18 is a plot of the 3047 noise system's floor in the DCFM mode of operation at 640MHz. In this mode the typical value at 1kHz offset is specified as -116bBc/hz [22]. At a frequency of 1040 MHz, this value may be even higher which raises some concern with using this method when evaluating overmoded filter based oscillators, and may have been masking the actual measured performance from section 5.3. Unfortunately, in initial tests, the EFC option of voltage controlled measurements was unable to maintain lock. This is a specific area that needs attention as this technique will become a necessity as oscillators employing higher Q filter sections are designed and tested.

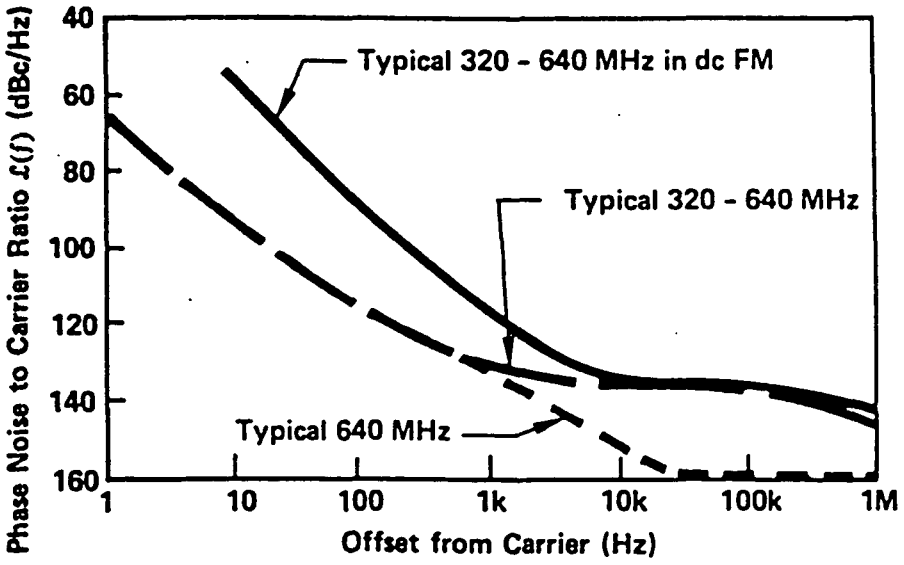


Fig. 5.18
Noise Floor of HP3047 System Using DCFM Method

6. CONCLUSIONS

6.1. Summary of Work

The purpose of this thesis was to report on the design and operation of TFR based oscillator circuits, and the characterization of the oscillators in terms of their individual components and overall closed loop performance. Some of the early work was reported in a paper titled "Non-Linear Modeling and Performance of Oscillators Using Thin Film BAW Devices," published in the Proceedings of the 42nd Annual Frequency Control Symposium, Baltimore, Maryland, 1988, which was authored by S. G. Burns, and co - authored by P. H. Thompson and G. R. Kline [12]. Since the presentation of this paper, many advancements in oscillator design, SCF modeling, and actual circuit performance have been achieved. A more complete approach to designing oscillators by considering the inherent nonlinear operation of the active device in the oscillator was adopted. A method of optimizing the equivalent circuit of the SCF was developed which allows for the accurate modeling of the filter's bandpass characteristic, insertion loss, shape factor, and parasitic effects including packaging effects.

In addition, a working VCO at a fundamental frequency of over 1 GHz employing a TFR based stacked crystal filter was demonstrated for the first time. The linearity of the VCO allowed for direct FM and PLL functions to be demonstrated. This suggests numerous potential applications in the communications field. Another first was the design of a selectable mode oscillator using the overmoded SCF structure. Past

work indicated that the overmoded filter could be employed to design highly stable, low noise oscillators, but it was not possible to isolate one mode of operation at a time. It was found that by introducing a degree of time delay into the circuit using an additional SCF, it was possible to select any given single mode, and to tune between adjacent modes. The functioning oscillator's measured phase noise was found to be comparable to any known TFR based oscillators to date.

In Chapter 5, the Leeson noise model for a feedback oscillator was presented. Also, a method of measuring open loop parameters was used to measure the open loop flicker noise coefficient (α) of TFR based filters. The measured open loop parameters were substituted in the noise model and were seen to agree well with the actual measured performance. By varying parameters, such as the loaded Q and the feedback network's insertion loss, different noise performance as predicted by the model was systematically observed and accounted for which demonstrates the validity of applying the noise model to TFR based oscillators.

6.2. Direction of Future Work

As mentioned, the demonstration of VCO operation leads to many potential applications. Continued work in this area could lead to the development of unique communication system architectures which take advantage of the TFR's size, performance, and potential for monolithic integration. In particular, the methods used to demonstrate PLL operation using the SCF based VCO could be applied to the overmoded filter based oscillator. The construction of a fully functional hybrid

PLL would be a natural extension to the work done to this point, and would represent a milestone on the way to full system integration. Also, as lower insertion loss filters become available, multiple section overmoded SCFs could be used in oscillator circuits with loaded Qs of 10,000 or greater at 1 GHz. The synthesis of composite structures with Q values of this magnitude, would result in lower noise oscillators than those studied to date. It is anticipated that the development of TFR based circuits will eventually lead to fully integrated TFR based systems, and that this work will be useful in defining the basics of TFR based oscillator design, applications, and performance.

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8. ACKNOWLEDGEMENTS

The completion of this work would not have been possible without the continued support and guidance of my major professor, Dr. Stanley G. Burns. In particular, Dr. Burns has been involved with the TFR based oscillator project from its inception and was instrumental in expanding upon earlier TFR based oscillator work to lead to the development of the circuits as reported. Other areas of contribution include active device modeling and SPICE simulation analysis. Another major contributor to this project was Dr. Robert J. Weber. Dr. Weber applied his expertise in making microwave measurements and circuit analysis. His method of measuring large signal S parameters was an integral part of the non-linear oscillator circuit analysis. Also Gary Kline was responsible for the actual packaging of the TFR based filters and for supplying filter samples whenever needed. Also, I wish to express my appreciation to my committee members, Drs. Alvin A. Read and Joseph Shinar for their commitment of time and energy.

I would like to thank Iowa State University, the Graduate College, and the Electrical Engineering Department for providing me with the opportunity to pursue the degree of Master's of Science; the Microelectronics Research Center for funding my research work and providing the facilities and equipment to make it possible; and Dr. Kenneth M. Lakin and the MRC staff.

The following companies donated either materials or use of equipment, and their contribution is also greatly appreciated: Rockwell

Collins, Cedar Rapids, Ia., for the use of their measurements lab; Keene Corporation, Bear, Del., for donating microwave laminates; Fair - Rite, Wallkill, N.Y., for donating ferrite beads; Alpha Semiconductor, Woburn, Mass., for donating varactor diodes; Mini Systems, Plainville, Mass., for donating device packages; and the Electronic Technology Corporation, Ames, Ia., for the use of its computers and drawing programs.

Lastly, I would like to thank my parents for their ever-present support, their high expectations, and for teaching me the value of honest work. It is to them that this work is dedicated.

9. APPENDIX A:

MICROSTRIP EQUATIONS, TECHNIQUES, AND MATERIALS USED

The oscillator circuits and device test fixtures were constructed on microstrip. The microstrip board was manufactured by Keene Corporation, Laminates Division. The 60 mil board is copper clad on both sides and has a dielectric constant, ε_r of 2.50 ± .05. The dimensions for a 50Ω transmission line were obtained from an application note supplied by Keene [23]. With a copper thickness of t = 1.4 mils and a line width of w = 174 mils, the approximate equations derived from conformal mapping techniques to account for fringing effects are satisfied [24].

(Fig. 9.1, Eqs. 9.1 through 9.3)

$$w_{eff} = w + \frac{t[1 + \ln(2h/t)]}{\pi} \qquad t/h \geq .005 \tag{9.1}$$

$$\varepsilon_{re} = (\varepsilon_r + 1)/2 + (\varepsilon_r - 1)(1 + 12h/w_{eff})^{-1/2} \qquad w/h \geq 1 \tag{9.2}$$

$$Z_o = \frac{120\pi}{[(\varepsilon_{re})^{1/2} \times (w_{eff}/h + 1.393 + 0.667 \ln(w_{eff}/h + 1.444))]} \tag{9.3}$$

The wavelength in centimeters may be calculated by:

$$\lambda_{eff} = \frac{300 \times 10^8}{(\varepsilon_{re})^{1/2} \times f} \tag{9.4}$$

where f is the frequency in hertz.

The pattern for designing the microstrip transmission lines may be transferred to the board by using photoresist and a mask under ultraviolet light, or in the case of relatively simple circuits, the board may be masked with plastic tape or black wax. The patterned circuit board is immersed in an etching solution of ferric chloride to remove the unwanted copper, the mask or photoresist is removed, and the board is thoroughly cleaned to insure solderability.

An appropriate bias network for high frequency amplifiers may be designed using quarter wave sections of transmission line. A high impedance path is desired in the operational bandwidth of the amplifier for the bias network which should in turn be of a relatively low impedance at D.C. Using a low Z_o of 15Ω open circuit line, one can show, using Eq. 9.5, that the impedance at an electrical length of 90° is essentially zero. If this line loads a second line with a high Z_o of 50Ω, then, using Eq. 9.6, at an electrical length of 90°, one can achieve an extremely high impedance in the frequency range where the line lengths are approximately one quarter wavelength long [24]. The dc bias is fed into the junction of the two lines through a 100Ω resistor to provide temperature stability and to limit current.

$$\text{Open Ckt. Line} \qquad Z_{in} = -jZ_o \times \cot(\theta) \tag{9.5}$$

$$\text{Short Ckt. Line} \qquad Z_{in} = +jZ_o \times \tan(\theta) \tag{9.6}$$

A typical bias network used in an amplifier test fixture is shown in Fig. 9.2. In most cases, a current mirror is preferable to a fixed

resistor in order to maintain a constant bias under various loading conditions, especially when the amplifier is used in a VCO application or when large signal measurements as described in Appendix C are taken.

The amplifiers used in the oscillator designs were manufactured by Mini Circuits. Table 9.1 lists the manufacturer's specifications for the MAR series of amplifiers. S parameter performance curves are shown in Fig. 9.3 [25].

Table 9.1 Amplifier Specifications

Model No. Color Dot	FREQ. MHz	GAIN, dB Typical (at MHz) 100	500	1000	2000	(Note 4) MIN	MAXIMUM POWER, dBm Output (1dB) Compression	Input (no damage)	DYNAMIC RANGE Intercept pt. dBm NF dB Typ.	3rd Order Typ.	VSWR In	Out	MAXIMUM RATING (25°C) I(mA)	P(mW)	DC POWER at Pin 3 Current (mA)	Volt. Typ.	PRICE $ Ea.	Qty
MAR 1 Brown	DC-1000	18 5	17 5	15 5	—	13 0	0	+10	5 0	15	1 5	1 5	40	100	17	5	0 99	(100)
MAR 2 Red	DC-2000	13	12 8	12 5	11	8 5	- 3	+15	6 5	18	1 3	1 6	60	325	25	5	1 50	(25)
MAR 3 Orange	DC-2000	13	12 8	12 5	10 5	8 0	▲- 8	+15	6 0	23	1 6	1 6	70	400	35	5	1 70	(25)
MAR 4 Yellow	DC-1000	8 2	8 2	8 0	—	7 0	-11	+15	7 0	27	1 9	2 1	85	500	50	5	1 90	(25)
MAR 6 White	DC-2000	20	19	16	11	9	0	+15	2 8	15	2 1	1 8	50	200	16	3 5	1 29	(25)
MAR 7 Violet	DC-2000	13 5	13 1	12 5	10 5	8 5	- 4	+15	5 0	20	2 1	1 5	60	275	22	4	1 90	(25)
MAR 8 Blue	DC-1000	33	28	23	—	19	+10	+15	3 5	27	⊏	⊐	65	500	36	7 5	2 20	(25)

NOTES:

▲ +4 dBm (1-2 GHz)

⊐ MAR-8 input and output impedances are not 50 ohms, see S parameter data Conditionally stable* for source/load VSWR - 3 1

1 Operating temperature -20°C to +85°C
Storage temperature -55°C to +100°C

2 With no load output, derate maximum input power (no damage) by 10dB

3 Price and specifications subject to change without notice

4 Minimum gain at highest frequency point and over full temperature range

* MAR-8, Input/Output impedance is not 50 ohms, see data sheet
Stable for source/load impedance VSWR less than 3:1

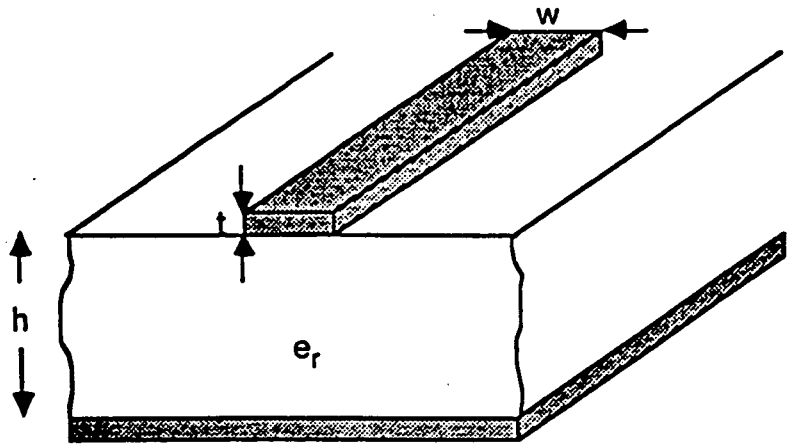


Fig. 9.1
Microstrip Cross Section

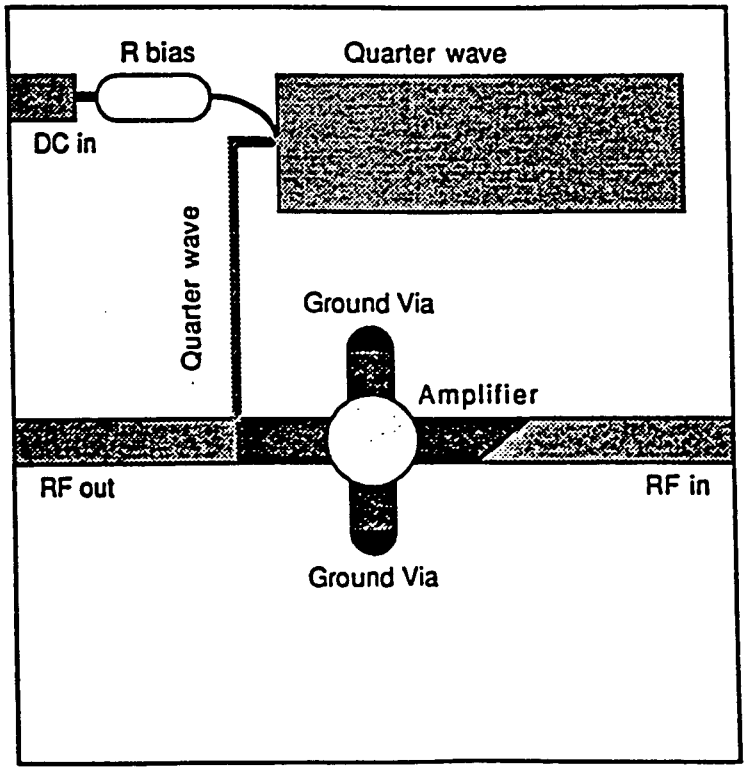


Fig. 9.2
Amplifier Bias Network

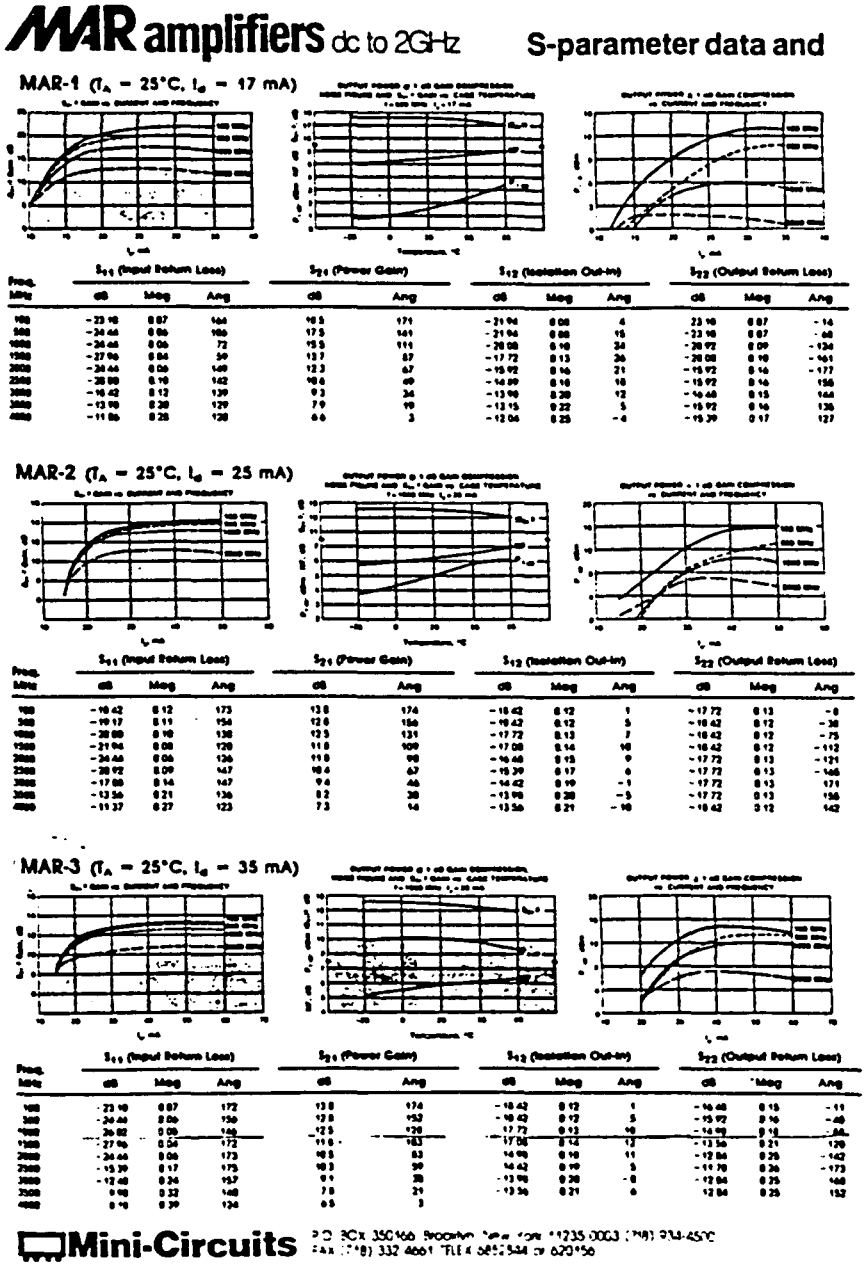
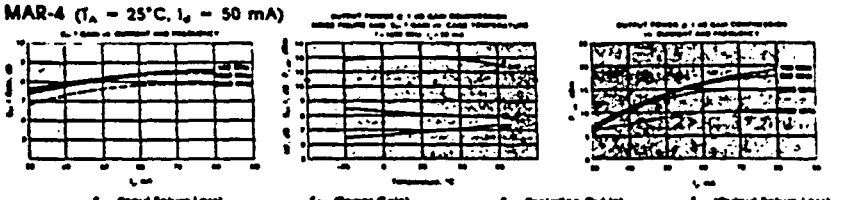


Fig. 9.3
Amplifier Performance Curves

performance curves

Mini-Circuits

MAR-4 (T_A = 25°C, I_d = 50 mA)

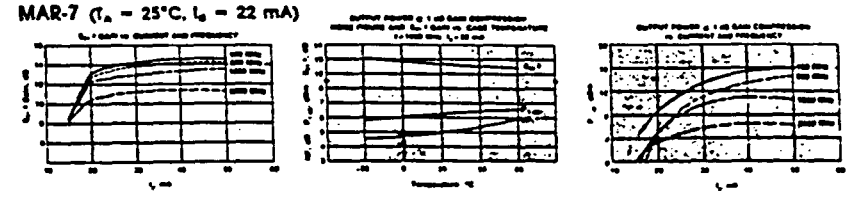


Freq. MHz	S_{11} (Input Return Loss) dB	Mag	Ang	S_{21} (Power Gain) dB	Ang	S_{12} (Isolation Out-In) dB	Mag	Ang	S_{22} (Output Return Loss) dB	Mag	Ang

MAR-6 (T_A = 25°C, I_d = 16 mA)

Freq. MHz	S_{11} (Input Return Loss) dB	Mag	Ang	S_{21} (Power Gain) dB	Mag	Ang	S_{12} (Isolation Out-In) dB	Mag	Ang	S_{22} (Output Return Loss) dB	Mag	Ang

MAR-7 (T_A = 25°C, I_d = 22 mA)



Freq. MHz	S_{11} (Input Return Loss) dB	Mag	Ang	S_{21} (Power Gain) dB	Ang	S_{12} (Isolation Out-In) dB	Mag	Ang	S_{22} (Output Return Loss) dB	Mag	Ang

Fig. 9.3 (continued)

10. APPENDIX B:

DETAILS OF SCF PACKAGING AND ASSOCIATED PARASITICS

The ultimate goal of designing circuits using TFR technology is to incorporate the resonator on the same substrate as the rest of the circuit. TFR devices may also be used as a discrete devices if they are appropriately packaged. In the past, resonators and resonator based filters have been mounted in a "U-Channel" to allow measurements to be conducted and to interface with external circuitry. Some of the configurations used are shown in Figs.10.1a and 10.1b. In Fig. 10.1a, the die containing the resonator device is mounted to a brass or aluminum piece of channel which essentially acts as a ground plane. The connection from the resonator to the center conductor of the SMA coaxial connector is accomplished by a wire bond of approximately a centimeter in length. This introduces a parasitic inductance of approximately ten nH, as well as a transmission line impedance mismatch at both ends of the wirebond. The wirebond is also very vulnerable to breakage from rough handling. Fig. 10.1b shows an improvement on the "U Channel" theme where the resonator device is encased in a TO type transistor can which is then soldered to the channel. Two of the TO package's leads are used to connect to the SMA center conductors. This approach reduces the inductance to some extent and provides for a more rugged device, but is still far from optimal in terms of size and impedance matching.

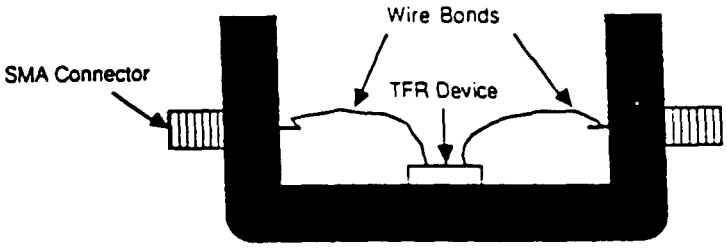


Fig. 10.1a
"U Channel" Device Mounting

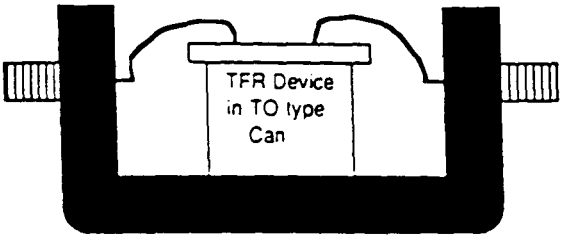


Fig. 10.1b
Improvement over Fig. 10.1a

Microstrip is commonly used above a few hundred megahertz to interconnect components and construct microwave filters and matching networks. In order to interface TFR devices with a microstrip circuit, a flat pack style package with a metal base (Mini-Systems Part # 5H10M-6) was employed as shown in Fig. 10.2. The packages were modified by eliminating all the leads except for the middle lead on opposing sides to accommodate the input and output ports to the resonator device. A resonator device mounted in a modified flatpack package is shown in Fig. 10.3. The packaged device drops neatly into a rectangular hole machined in the microstrip board with the Metal back of the package lining up with the board's ground plane, and the leads lining up with the transmission lines patterned on the top of the board. The input and output of the resonator are accessed by short wire bonds approximately 2 mm in length and the ground is accessed by multiple wirebonds to the metal back of the package which in turn is connected to the ground plane of the circuit board by a strip of copper foil.

The inductance of the wirebonds as well as the capacitance of the package can be accounted for with the inclusion of these parasitics in the equivalent circuit model. Fig. 10.4 shows how the parasitics of the package may be included external to the embedded two port model of the resonator device to obtain the resulting two port model at ports 1' and 2'. L_{WB1} and L_{WB2} are artifacts of the lead inductance of the wirebonds and can be estimated by using 20nH/inch as a guideline. Typically a range of 1 to 4 nH will be used in the Touchstone optimization routines with final optimized values of approximately 1.8nH. L_G is a result of

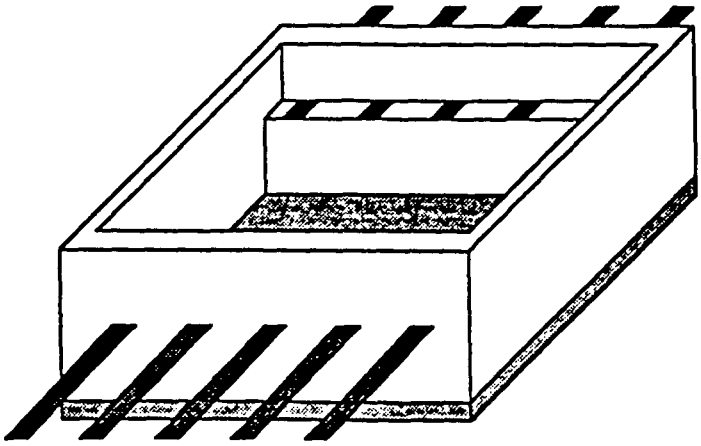


Fig. 10.2
Mini Circuits Leaded Flatpack

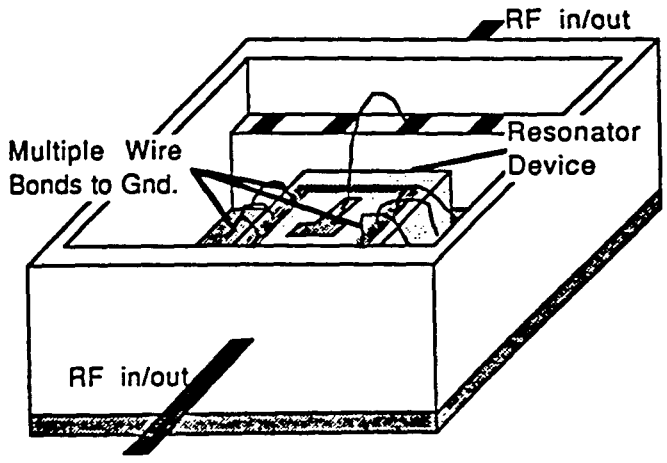


Fig. 10.3
Mounted TFR Device

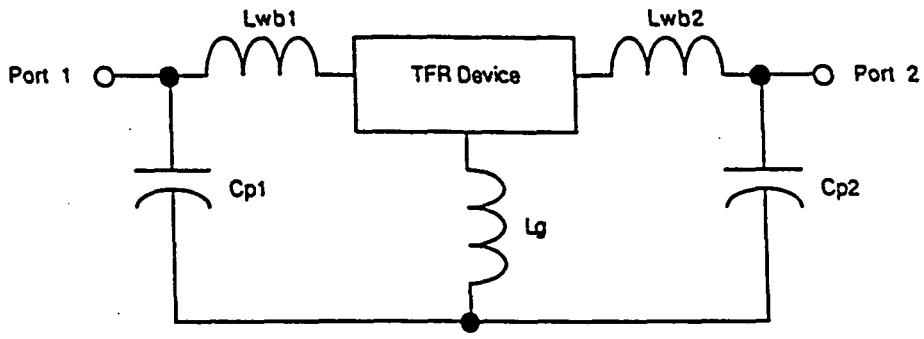


Fig. 10.4
Modeling of Parasitics

the nonideal path to the ground plane. Its effect is reduced by increasing the number of bonds to ground and falls into the range of a few hundredths of a nH. C_{P1} and C_{P2} account for the capacitive change in the dielectric package as well as any stray capacitance from the wirebond to ground. This value may be approximated roughly as a parallel plate capacitor with dimensions defined by the package thickness and lead width. This capacitance is typically less than a tenth of a pF and can be included as an optimized parameter as well.

Resonator devices packaged by these methods exhibit performance superior to those mounted in "U-Channel" especially in terms of out of band rejection with an improvement of 15 to 20 dB. Figs. 10.5a and b show the effects of the package parasitics on the performance of a series stacked crystal filter as mounted in a "U-Channel" and as packaged in a leaded flatpack, respectively. This allows for a comparison between the old and new packaging methods.

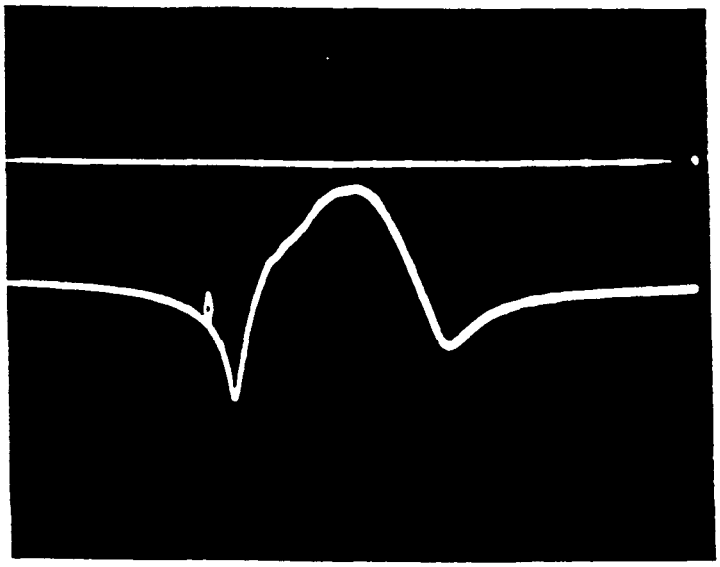


Fig. 10.5a
Performance of "U Channel" Mounted Device

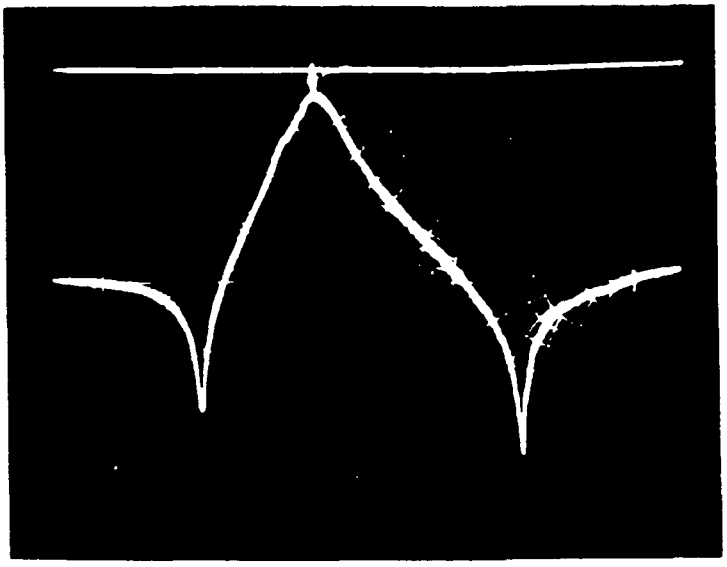


Fig. 10.5b
Performance of Packaged Device

11. APPENDIX C:

LARGE SIGNAL S PARAMETER MEASUREMENTS

Network analyzers such as the HP8505 using the HP8503 S Parameter Test Set are designed to take small signal measurements. In order to take large signal measurements, a large signal, enough to drive the DUT into compression, must be present at the input port at all times. The HP8503 provides this signal only when S_{21} and S_{11} are being measured, while S_{22} and S_{12} are measured with the input port terminated in a 50Ω load. The following perturbational method for computing the large signal S parameters as developed by Dr. R. J. Weber is presented in condensed form.

Consider the measurement setup in Fig. 11.1. The parameters S_{21} and S_{11} may be measured directly using Eqs. 11.1 and 11.2.

$$S_{21} = b_2/a_1\big|_{a2 = 0} \tag{11.1}$$

$$S_{11} = b_1/a_1\big|_{a2 = 0} \tag{11.2}$$

In this case, the external hardware is duplicating the function of the HP8503 S Parameter Test Set. Now if the measurement setup is modified as in Fig. 11.2a and b with two different loading conditions corresponding to Γ_L and Γ_{L*}, then S_{12} and S_{22} may be measured while maintaining power at port 1. It can be shown that for two separate loading conditions corresponding to Γ_L and Γ_{L*}, that S_{12} and S_{22} may be expressed as

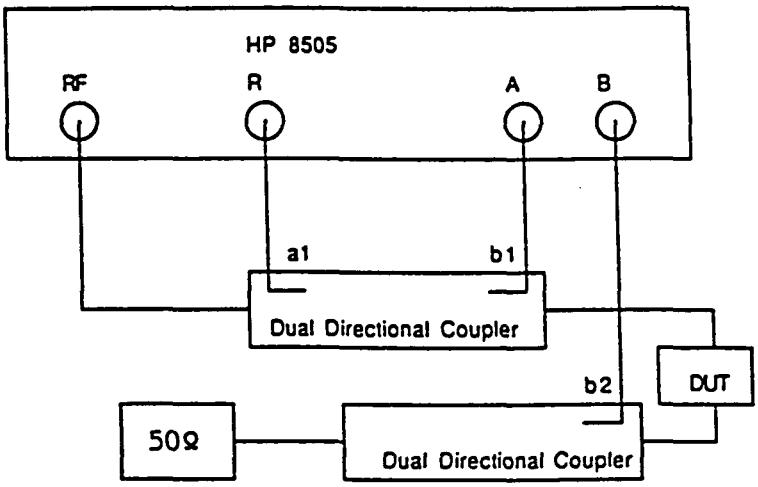


Fig. 11.1
Measurement Setup for S_{11} and S_{21}

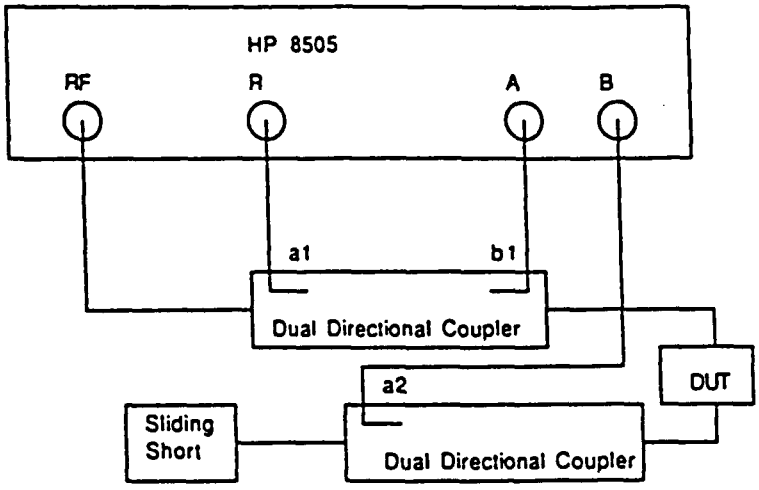


Fig. 11.2a
Measurement Setup for S_{12}

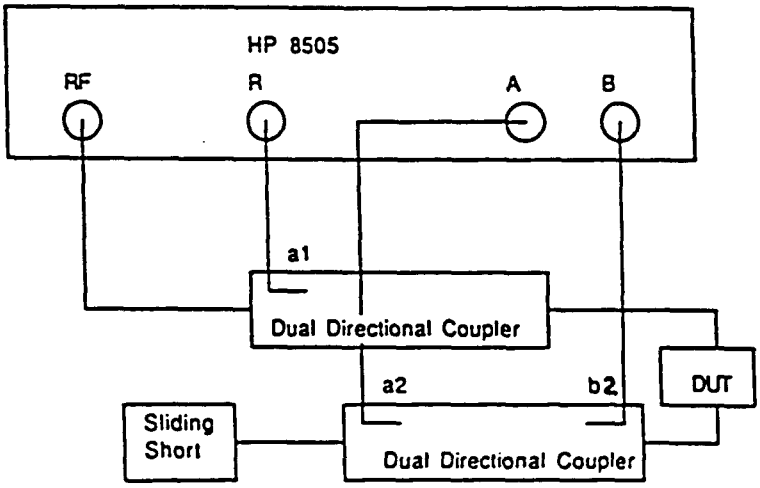


Fig. 11.2b
Measurement Setup for S_{22}

$$S_{12} = \frac{B_1 - B_{1*}}{A_2 - A_{2*}} \tag{11.2a}$$

$$S_{22} = \frac{B_2 - B_{2*}}{A_2 - A_{2*}} \tag{11.2b}$$

where $B_1 = b_1/a_1$, $B_2 = b_2/a_1$, $A_2 = a_2/a_1$, etc. When displayed in a polar form, the signals of B_1, B_2, A_1, A_2, etc., will trace out a circle as the load is continuously changed. If we write the equation of two circles as

$$A_n = R_{an} + \rho_{an}\exp[i(\phi_{an} + \phi_{on})] \tag{11.3a}$$

$$B_n = R_{bn} + \rho_{bn}\exp[i(\phi_{bn} + \phi_{on})] \tag{11.3b}$$

then the resulting expressions for S_{12} and S_{22} may be derived [17].

$$S_{22} = \frac{\rho_{b2}\exp(i\phi_{b2})}{\rho_{a2}\exp(i\phi_{a2})} \tag{11.4a}$$

$$S_{12} = \frac{\rho_{b1}\exp(i\phi_{b1})}{\rho_{a2}\exp(i\phi_{a2})} \tag{11.4b}$$

The task reduces to taking the ratio the radii of the two circles as the load is changed, and the difference in relative phase between the two circles for any given load condition. A pen plotter was connected to the rear panel of the network analyzer to record the measurements. A plot used in computing S_{22} is shown in Fig. 11.3. The crosses indicate the points where the relative phase was determined. As the device compresses, the circular plots become oblong corresponding to the

nonlinearities present when a device is driven into gain compression. The resulting large signal S parameter measurements for the amplifier used in the VCO example at various input power levels are given in Table 11.1.

Table 11.1 Large Signal Measurements on VCO Amplifier

P_{in} dBm	S_{11} dB @ °	S_{12} dB @ °	S_{21} dB @ °	S_{22} dB @ °
-30	-19.2 107	-18.9 49	15.7 96	-17.2 151
-20	-19.2 109	-18.9 49	15.7 96	-17.2 156
-10	-21.8 107	-18.9 49	15.6 96	-17.5 161
-5	-31.1 71	-17.6 49	15.1 98	-18.1 181
0	-12.7 -59	-14.2 54	11.9 104	-5.4 -4
5	-9.5 -48	-13.1 54	8.4 101	-4.3 -4
10	-8.4 54	-8.9 54	3.4 95	-4.5 -4

MAR 6 AMP @ 1040 MHz
I = 25 mA
Incident Power = -10 dBm

10/10/88
Measurement S22

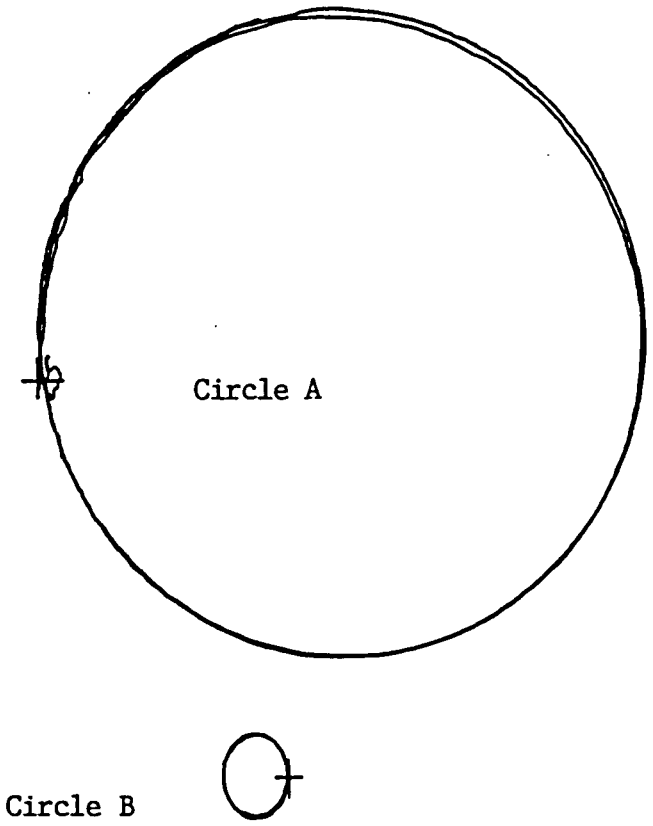


Fig. 11.3
Large Signal S_{22} Plot