A microcomputer-based digital ultrasonic system

by

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1. INTRODUCTION

The ultrasonic pulse echo technique has achieved a wide spread acceptance in medical diagnosis and there are a variety of machines commercially available. The information obtained from the pulse echo signal is the amplitude, frequency, phase and transmission time delay. This information has been processed to determine properties of many tissues.

Systems developed in recent years have been successful in determining the properties of many tissues using pulse echo ultrasound. The flexibility of programming and the computation in a digital computer are most important in the quantitative analysis of the reflected ultrasonic signal. If these systems can be implemented on an inexpensive microcomputer or microprocessor system, the analysis of the returned ultrasound signal can be performed on a real time basis.

The processing of the reflected ultrasonic pulse echo can be for amplitude shaping, signal filtering, signal to noise ratio improvement and data rearrangement.

The primary objective of this thesis was to design and build an inexpensive microcomputer controlled interface system capable of sampling, storing and analyzing the reflected ultrasonic pulse. The stored data should give both the amplitude and phase information of the echo signal.

A simplified block diagram of the system is shown in Figure 1. The microcomputer is Intel 8052AH 8-bit microcomputer. The pulser which produces the pulse to trigger the transducer is triggered by the signal from the microcomputer. The reflected echo signal from the transducer is amplified by a video amplifier to match the input specifications of the

A/D converter. The signal is digitized by an RCA CA3300 A/D Flash converter at a rate of 2 MHz. An overall sampling rate of 8 MHz is achieved by repetitive sequential sampling. Due to the need of this high speed data acquisition and relatively low speed of the microcomputer an intermediate storage circuitry was implemented.

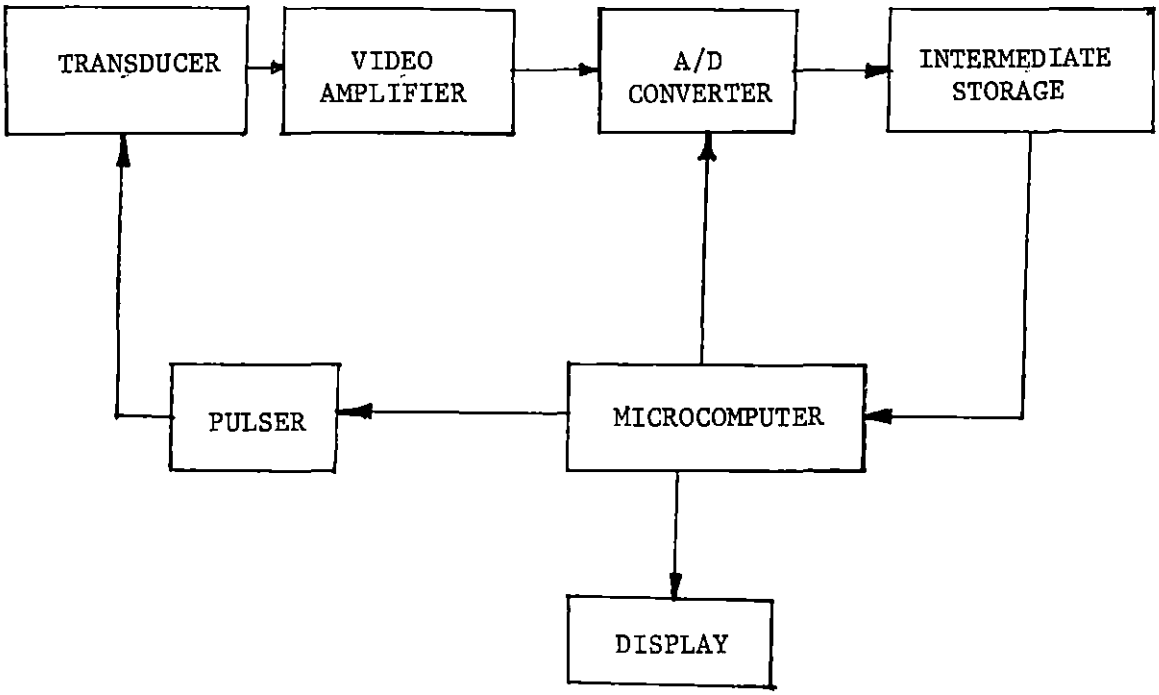

FIGURE 1. Block diagram of the system

The intermediate storage has a total capacity of 8x8 Kbytes of memory. The control signals to the A/D converter and the intermediate memory to achieve this sampling rate are derived from the outputs of a 4-bit binary counter which is fed by an 8 MHz master clock. The counter is controlled by the microcomputer. The stored data are transferred into the main memory of the computer. The digitized values of the stored

signal can be viewed on a computer terminal, where upto 70 locations can be viewed at a time. Alternatively the data can be sent to a digital to analog converter connected to the computer and the signal can be viewed on an oscilloscope.

2. BACKGROUND

First practical application of the pulse echo technique was developed by Langevin in 1916 for submarine detection. In the late 1930s and 1940s ultrasound was applied to solve industrial problems. As mentioned by Wicks, Firestone's instrument utilized the pulse echo principle to detect flaws in metals. Using this early industrial equipment the first medical researchers began their search for possible medical applications. Woodcock mentioned that Fry et al. (1968) were the first to describe a pulse echo acquisition system with computer control both of the scanning aspect and analog signal processing which could be digitally controlled.

Many pulse echo acquisition systems under computer control have been developed. A dedicated general purpose pulse echo instrument called DONAR was built by Lees et al. (1974) and provides many functions. It can sample and record digital ultrasonic data, select and extract only the desired information and display the processed data. It is dedicated mainly for pulse echo signals. The central unit of DONAR is a Digital Equipment Corp. (DEC) PDP 9/L computer. A 20 MHz crystal serves as a master clock. A suitable number selected by the operator is transmitted under program control to a register in the sampling rate countdown timer which sets the sampling rate. The maximum real time sampling rate is 10 KHz. With a pulse repetition process the effective sampling rate can be selected from 40 MHz to 20 GHz. DONAR can work as an amplifier, differential amplifier, timing gate amplifier and display unit.

Goldstein et al. (1975) have produced a system known as CUPAD, for computerized ultrasound acquisition, processing and display. The computer is a DEC PDP-15. It employs a 6-bit A/D converter to digitize the reflected ultrasonic signal. The signal is stored, processed and displayed. An interactive system for processing pulse echo signals was built by Robison et al. (1976). It uses a Interdata Model 80 minicomputer and a peripheral microprocessor system for its function. 6 MHz sampling rate is used to sample 2 MHz ultrasonic pulses. Acquisition of the echo signal is controlled by the microprocessor and storage and processing by the Model 80 minicomputer. Here, the systems data acquisition rate is limited by the speed of the direct memory access port provided by the Model 80's memory controller, which has an average transfer rate of 3 million 16-bit accesses/sec. Two 8-bit samples are packed into 16-bit value in one memory cycle to achive 6 MHz sampling rate. It is shown that this sampling rate retained magnitude and frequency information of the pulse echo signal.

The analysis of the ultrasonic signals in diffuse liver desease was done using a minicomputer system by Lerski et al. (1979). Study of alchohol induced diffuse liver desease was done using a combination of amplitude and texture analysis of recorded pulse echo signals. The reflected 2.5 MHz pulse echo signals are digitized at a rate of 20 MHz/8bits word and stored in a intermediate memory (4 Kbytes) and later transferred to a Data General NOVA3 minicomputer. Most of the controlling is done using an assembly language subroutine, called by the main Fortran program. This system worked satisfactorily for the alcohol induced diffuse liver disease research.

Measurement of attenuation and dispersion in solids was done by Kline (1984). Here, a Panametrics 8052 pulser-receiver was used to excite the transducer and to amplify the reflected acoustic signal, a Biomation 8100 digitizer was used for analog to digital conversion and the data were stored in DEC PDP 11/23 computer. The Biomation 8100 has a maximum sampling rate of 100 MHz.

Botros et al. (1984) have developed a high speed (16 MHz) analog to digital conversion system to interface with a IMS International microcomputer for the tissue characterization study. They used an Advanced Technology MK500 system to excite the transducer and also to amplify before the analog to digital conversion. A TRW TDC 1025 analog to digital converter used. The TDC 1025 is ECL compatible and its digital outputs are converted to TTL levels. The control lines for the intermediate memory is derived from a master clock and control delay circuitry.

Glueck et al. (1985) have developed a system to measure changes in ultrasonic attenuation and backscatter of muscle with change of contraction. They used a Metrotec MP215 pulser, which can give sine wave bursts of 4 usec duration of 2-9 MHz frequency. The reflected signal from the Panametric V309 broad band 5 MHz center frequency transducer is sampled, and stored in a Hewlett Packard 9825T computer.

Bronez et al. (1985) have developed a system to measure the ultrasound velocity in biological tissues using a Z-80 microprocessor based system. The STD bus of this processor can be interfaced to communicate with other systems. The ultrasound velocity was measured as a function of the temperature and frequency. The principle involved in measuring the velocity is by measuring the transmission delay. A Fluke counter

(model 7260A) controlled by the microprocessor is triggered by the transmitting pulse and stopped by the received pulse. They have determined the effect of temperature and frequency on the ultrasound velocity in bovine heart, kidney, liver and blood using this system.

3. SYSTEM DESCRIPTION

An ultrasonic data acquisition system was designed using an already fabricated Intel 8052AH microcomputer, purchased from Micromint, Inc.[1]

This computer system consists of an Intel 8052AH BASIC microcontroller chip, 32 kbytes of RAM, 2764/27128 EPROM programmer and three 8-bit parallel I/O ports. The 8052AH has a BASIC interpreter resident in its 8K ROM. The 8052AH also supports assembly language. The advantage of using assembly language is its high execution speed relative to the BASIC. The programs written in assembly language can be executed by using the call instruction in BASIC.

An interface system was designed by the author and added to this computer. The interface system system provides a pulse generater, a video amplifier, an analog to digital converter, an intermediate digital data storing system and a digital to analog converter. A detailed block diagram is shown in Figure 2.

A triggering pulse generated at a computer output port was sent through the delay-multiplexer circuit to the pulser. This causes the generation of a pulse which excites the transducer. The delay-multiplexer circuit was used to achieve a net sampling frequency of 8 MHz from an actual sampling frequency of 2 MHz. Figure 11 shows the function of the delay-multiplexer circuit. Figure 11 shows the methodology used to achieve a net sampling frequency of 8 MHz from an actual sampling frequency of 2 MHz.

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[1] Cost $239.00, The Micromint, Inc., 561 Willow Ave., Cedarhurst, NY 11516.

In response to the triggering pulse from the pulser, the transducer is shock excited into oscillation, producing a very high frequency acoustic damped pulse. This pulse signal is reflected back from a target and the transducer acting in a reciprocal mode produces an equivalent electrical voltage. This voltage signal from the transducer is in the order of millivolts and is amplified by a video amplifier to produce sufficient voltage for the A/D flash converter where the signal was sampled and converted into the equivalent digital value. The digitized data are sent to an intermediate memory.

The intermediate memory is connected to both the computer bus and the data sampling system. During the sampling procedure the computer bus must be isolated from the intermediate memory and during data reading and data transferring from the intermediate memory, its lines from the data sampling system must be isolated. Tristate buffers and bidirectional switches are connected to these lines to achieve the isolation.

The speed at which signal is sampled and digitized by the A/D converter and stored in the intermediate storage is independent of the computer speed. The control signals which are sent to the A/D converter to initialize sampling and analog to digital conversion, to the intermediate storage for the data storage and to the address generater counters to generate the address for the intermediate storage are derived from an 8 MHz master clock. The master clock signals are divided and decoded using 4-bit binary counters to produce address signals during the data storage. Stored data in the intermediate storage are transferred to the computer main memory using the computer control bus and the address bus connected through the tristate buffer and the data bus connected through the

bidirectional switches to the intermediate memory. The computer program is written in BASIC and assembly language. The BASIC program initializes the computer I/O ports, resets the counters and calls the subroutines written in assembly language where high execution speed is necessery. An assembly language subroutine, Sampler shown in Appendix C was called by the BASIC program to generate a trigger pulse, to excite the transducer, to initialize the sampling procedure and A/D conversion and to store the data in the intermediate memory. A second, assembly language subroutine Data-Mov, was called by the BASIC program to transfer the stored digital data from the intermediate memory to the main memory, which resulted an effective sampling rate of 8 MHz. The stored signal can be displayed either on an oscilloscope by sending the stored data to the D/A converter or on the computer terminal using software.

An effective sampling rate of 8 MHz from an actual sampling rate of 2 MHz is achieved by triggering the pulser four times successively, with a delay of 0, 124, 240 and 364ns, respectively. The same sampling procedure was maintained each time. Figure 10 shows the above methodology. This method is known as repetitive sequential sampling.

The system can be divided as follows:

1. Pulser
2. Receiver
3. Analog to Digital Converter
4. Microcomputer
5. Data Acquisition and Storage

Figure 2. A detailed block diagram of the system

Q1 2N3414 NPN silicon transistor

IC 1 LM733 Differential video amplifier

IC 2 CA3300 Flash A/D converter

IC 3, 7 MM74HC241 Octal tristate buffer

IC 4 HM62641p-15 8192 x 8 Static RAM

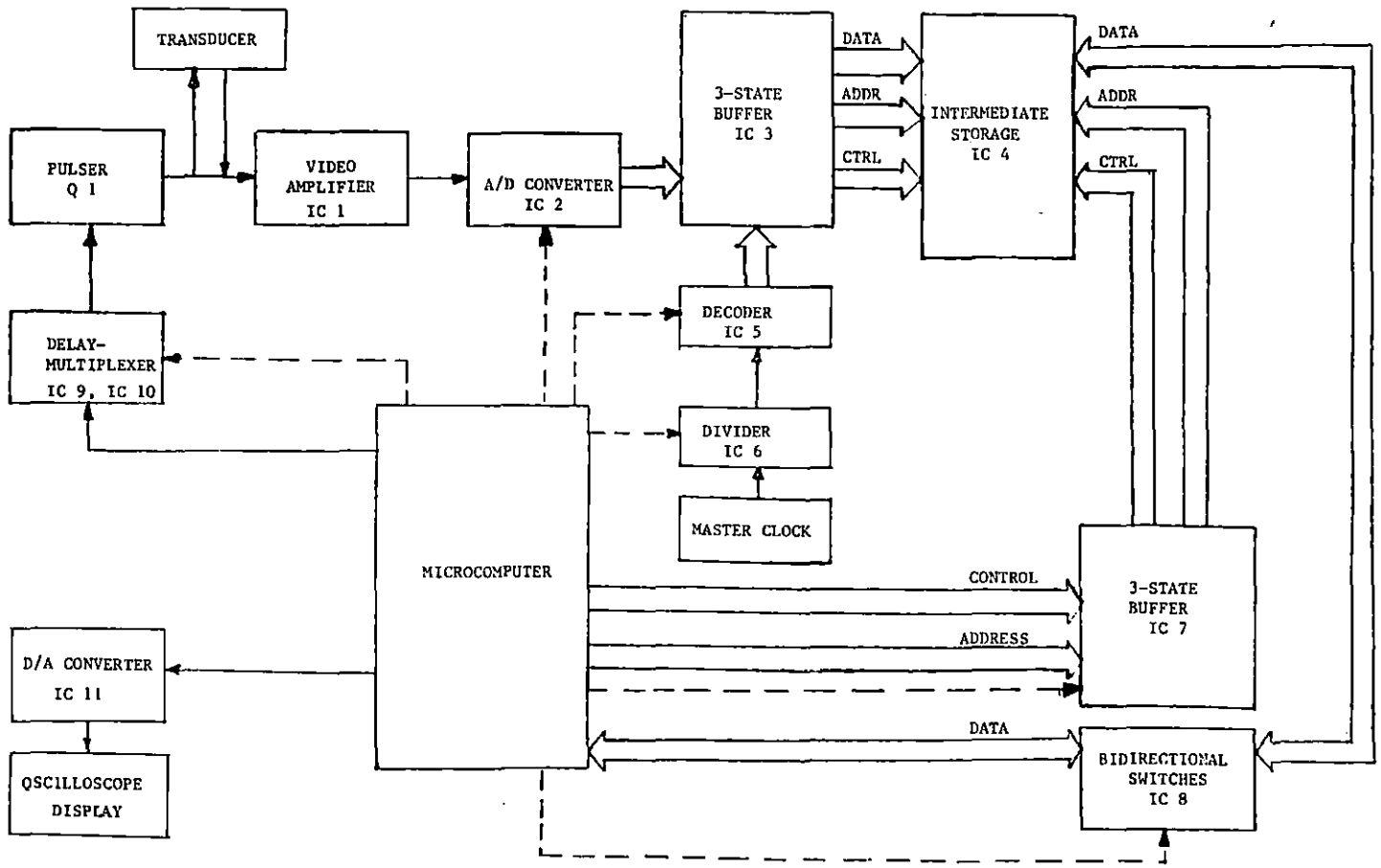
IC 5, 6 MM74HC161 4-bit Synchronous binary counter

IC 8 MM54HC4066 Quad bilateral switch

IC 9 MC14011 Quad 2-Input CMOS NAND gate

IC 10 MM74LS153 Dual 4-Channel multiplexer

IC 11 DAC808 8-bit digital to analog converter


TRANSDUCER
PULSER
Q 1
VIDEO
AMPLIFIER
IC 1
A/D CONVERTER
IC 2
3-STATE
BUFFER
IC 3
DATA
ADDR
CTRL
INTERMEDIATE
STORAGE
IC 4
DATA
ADDR
CTRL
DECODER
IC 5
DELAY-
MULTIPLEXER
IC 9, IC 10
DIVIDER
IC 6
MASTER CLOCK
MICROCOMPUTER
CONTROL
ADDRESS
3-STATE
BUFFER
IC 7
D/A CONVERTER
IC 11
DATA
BIDIRECTIONAL
SWITCHES
IC 8
OSCILLOSCOPE
DISPLAY

6. Digital to Analog Conversion and Display

7. Program and Control

3.1. Pulser

The pulser generates the transmitting pulse to excite the transducer. The circuit diagram of the pulser is shown in Figure 3. It was constructed using a 2N3414 npn transistor. The transistor is turned on by the leading edge of a pulse from PA7, a parallel I/O pin from the computer board. The switching action of the transistor causes discharging of capacitor C2, and the net result is a -5 volts negative pulse at A in the circuit shown in Figure 3. The width of the pulse depends on the smaller of the two time constants, R1C1 and R2C2. The R1C1 (R1=1K, C1=150pf) time constant was selected such that it is smaller when compared with that of R2C2 (R2=1K, C2=.1uf). So R1 and C1 values control the pulse width. With R1 and C1 values of 1K ohms and 150 pf, a -5 volts pulse with a width of 230 ns at A, gave a maximum voltage response in a RENCO 2.25 MHz transducer (Serial #3347). The R1 and C1 values can be changed if a different transducer which has different frequency response is used.

3.2. Receiver

The same transducer acts both as transmitter and receiver. The circuit diagram of the receiver is shown in Figure 3. The reflected ultrasonic signal was received and converted into its electrical equivalent by the transducer. The output of the transducer is in the order of millivolts and it is amplified by the National LM733 video amplifier. The input of the video amplifier is protected by the two diodes D1 and D2

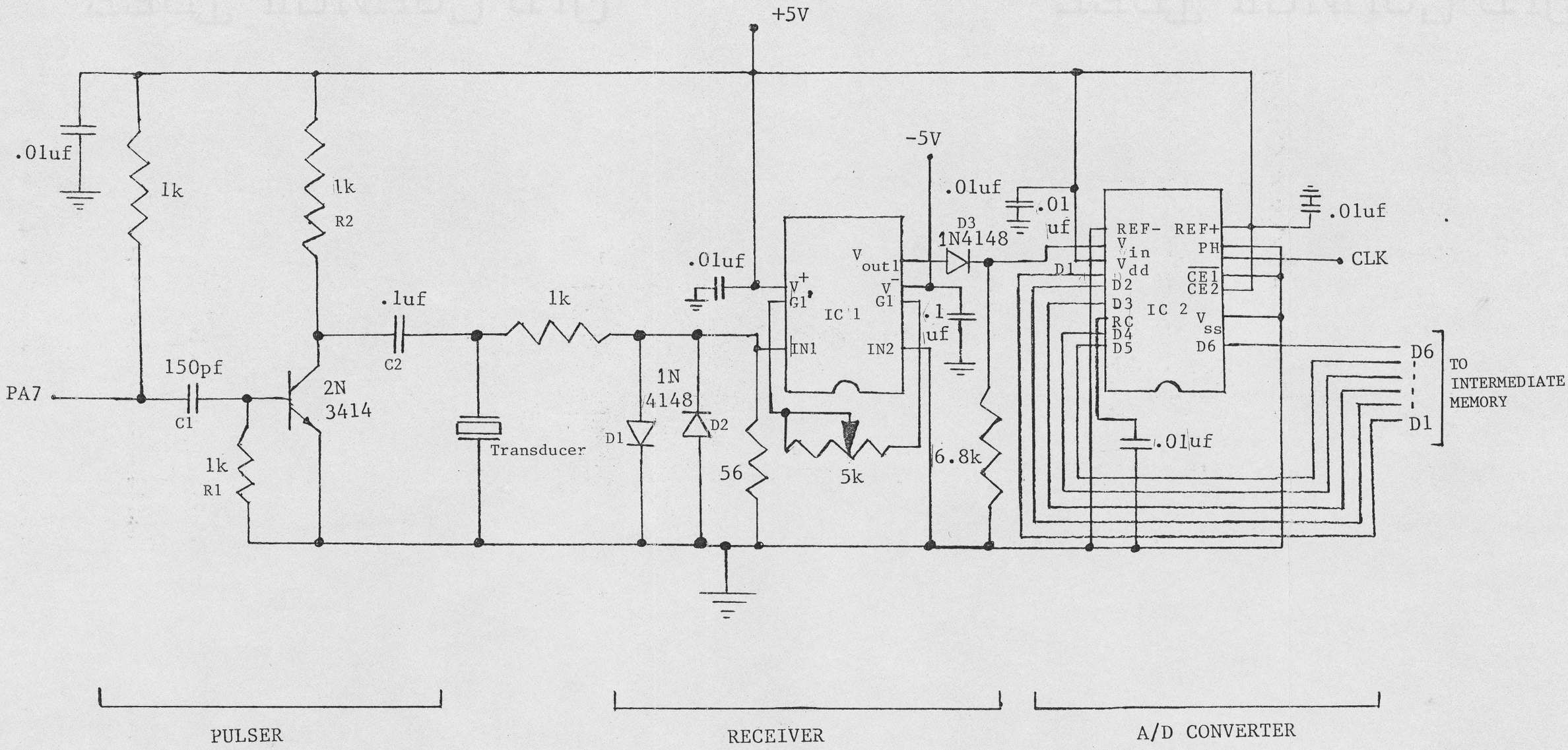


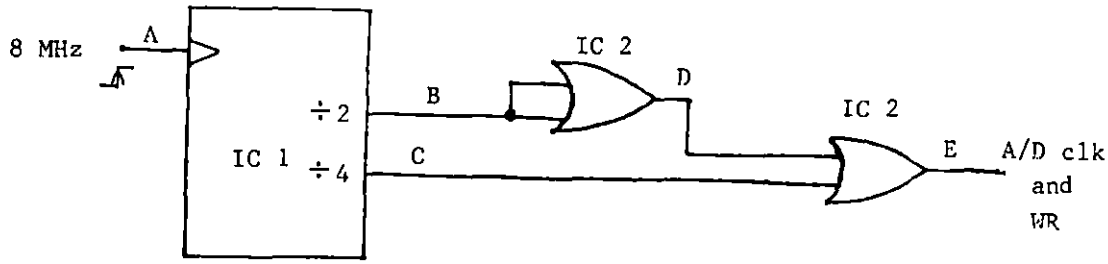
FIGURE 3. Pulser, receiver and A/D converter

connected as shown in Figure 3. Diodes D1 and D2 limit the input voltage of the video amplifier not to exceed 0.6 volts. For the present work, the selected gain range was 1 - 400. A 5K ohms potentiometer is connected between the gain select pins G1 and G1'. Using the potentiometer the gain of the video amplifier can be varied between 1 - 400. The gain of the amplifier was adjusted such that its output will not exceed the input range of the CA3300 A/D Flash Converter and also the entire dynamic range of CA3300 was utilized.

3.3. Analog to Digital Converter

Analog to digital conversion is done by the RCA CA3300 6-bit A/D Flash Converter. The circuit diagram of the analog to digital conversion stage is also shown in Figure 3. The CA3300 has a maximum sampling rate of 15 MHz. In the present work, 2 MHz was used as the actual sampling rate. CA3300 has 64 paralleled auto balanced voltage comparators which compares the input analog voltage with respect to the references Ref- and Ref+. The output of the comparators are decoded by a high speed logic circuitry and ouputs 6 bit binary equivalent of input analog signal. The operation of CA3300 has two phases, phase 1 "auto-balance" and phase 2 "sample unknown". The phase select pin, pin 8 is set logic low, such that phase 1 operation will be during logic high and phase 2 operation will be during logic low.

The reasons for selecting the logic level at pin 8 low are as follows:



IC 1 MM74HC161 4-Bit Synchronous Binary Counter
IC 2 MM74LS32 Quad 2-Input OR Gate

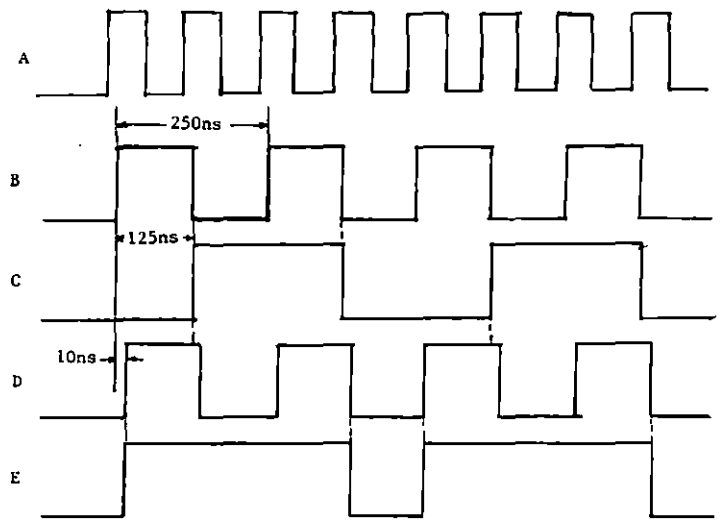


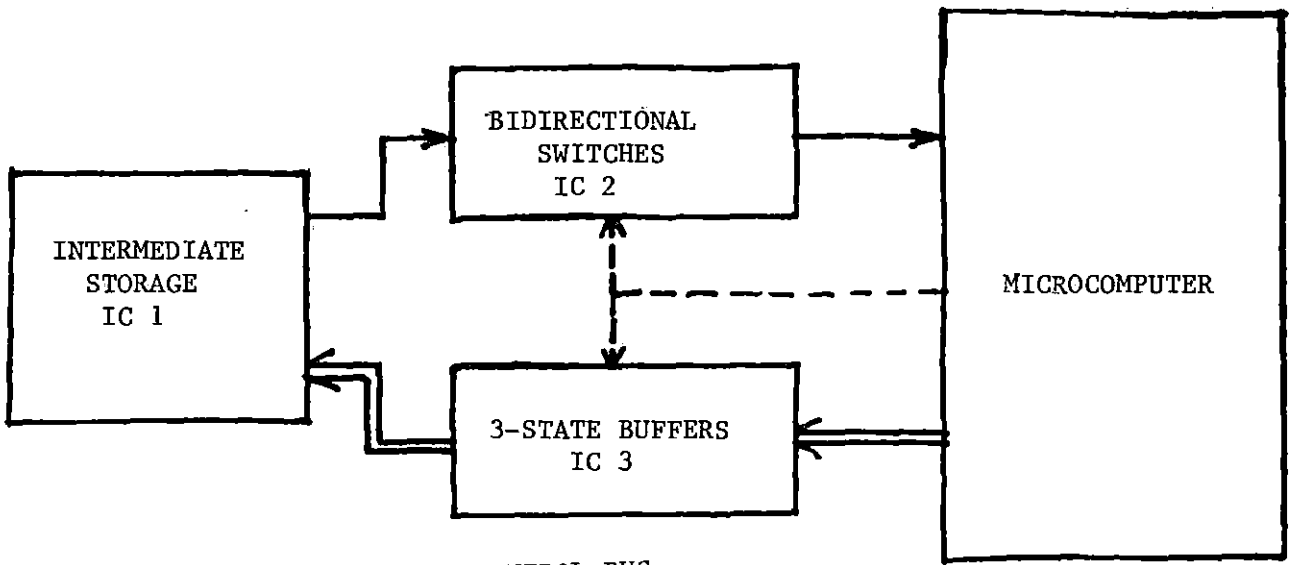
FIGURE 4. Generation of the control signal for A/D conversion and data write (a) circuit diagram and (b) timing diagram

1. The same control signal used for the clock of CA3300 can be used for the WR pin in 6264 buffer memory.
2. There was minimum delay between the end of digital conversion and write in the memory, so that the error caused by the drooping of the commutating capacitors in CA3300 was minimized.

Diode D3 connected as shown in Figure 3 protects the A/D converter by blocking any negative voltage entering its input. The circuit and timing diagrams for the generation of the clock signal sent to pin 7 are shown in Figure 4. The 4 MHz signal from the output of the divider of the master clock is delayed by 10 ns and ORed with 2 MHz signal from the divider. The resulting signal has high and low periods suitable for the required operation of the CA3300. The signal which has a low period of 125 ns used for WR signal in intermediate memory.

3.4. Microcomputer

The microcomputer board is a Micromint BCC52. This computer system consists of an Intel 8052AH BASIC microcontroller chip, 32 kbytes of RAM, 2764/27128 EPROM programmer and three 8-bit parallel I/O ports. The Intel 8052 has 16 bit address and 8 bit data bus, similar to common 8085 or Z80 microprocessors. Three most significant address bits were decoded by a 74LS138 decoder, so that the external addressable 64K bytes were separated into eight 8 Kbyte memory segments. Memory locations from 2000H-3FFFH, 4000H-5FFFH and 6000H-7FFFH were provided on the board. The EPROM addressed on the computer board uses locations 8000H-9FFFH. By selecting jumper options, locations 2000H-7FFFH can be selected for either program or data memory. An assembly language program is

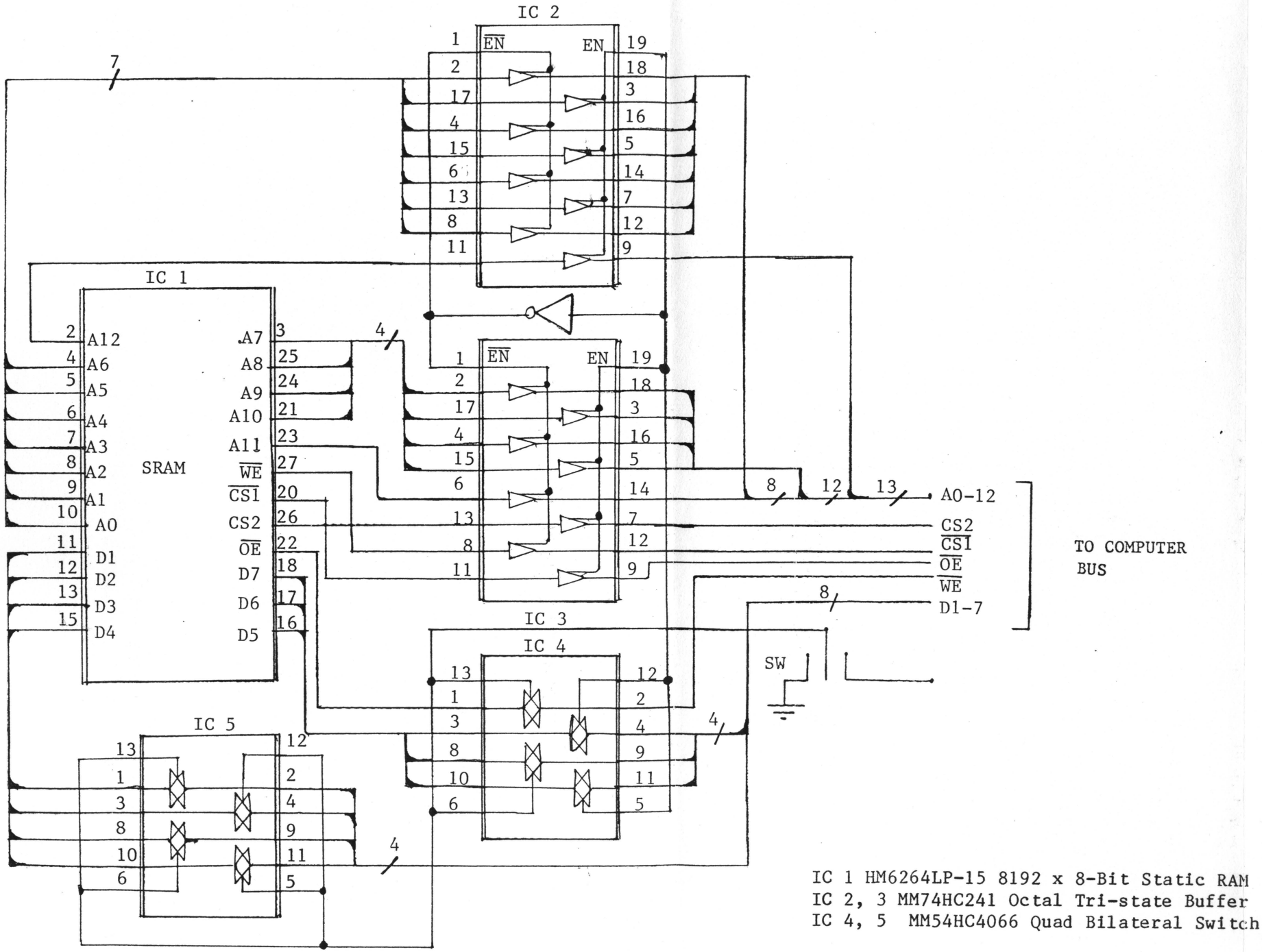


IC 1 HM6264lp-15 8192 x 8 Static RAM

IC 2 MM54HC4066 Quad bilateral switch

IC 3 MM74HC241 Octal tristate buffer

FIGURE 5. Block diagram of the computer interface with the intermediate storage



IC 1 HM6264LP-15 8192 x 8-Bit Static RAM
IC 2, 3 MM74HC241 Octal Tri-state Buffer
IC 4, 5 MM54HC4066 Quad Bilateral Switch

FIGURE 6. Circuit diagram of the computer interface with the intermediate storage

executable only if it is written in program memory. An expansion package for the BCC52 was purchased from Micromint, Inc. It is provided in a 2764 ROM. It should be placed in data memory. So for the present work, locations 2000H-7FFFH were set for data memory. This package provides a full resident assembler, a text editor to use with the assembler and some additional commands. Assembly language programs are assembled using this package.

The block diagram and circuit diagram of the interface between the computer lines and intermediate storage (6264) are respectively shown in Figure 5 and Figure 6. The decoded address, data and control lines for the data acquisition interface were directly taken through a socket provided for a 6264 SRAM that can be addressable at location 4000H-5FFFH. The address and control lines were connected through 74HC241 tristate buffers and data lines through 54HC4066 bidirectional switches.

3.5. Data Acquisition and Storage

The A-mode ultrasonic pulse echo data are in the form of bursts of radio frequency signals. The amount of memory required to hold a complete echo depends on the gating time. The center frequency of the transducer used is 2.25. The signal produced by the transducer due to the ultrasonic pulse was digitized at 8 MHz.

The block diagram and the circuit diagram of the data acquisition board is shown in Figure 7 and Figure 8 respectively.

The memory used for intermediate storage of the digitized data was Hitachi HM6264LP-15, 8x8 Kbyte static RAM. Its minimum access time is 150 ns. An 8 MHz master clock was connected to a binary counter which

Figure 7. Block diagram of the data acquisition interface

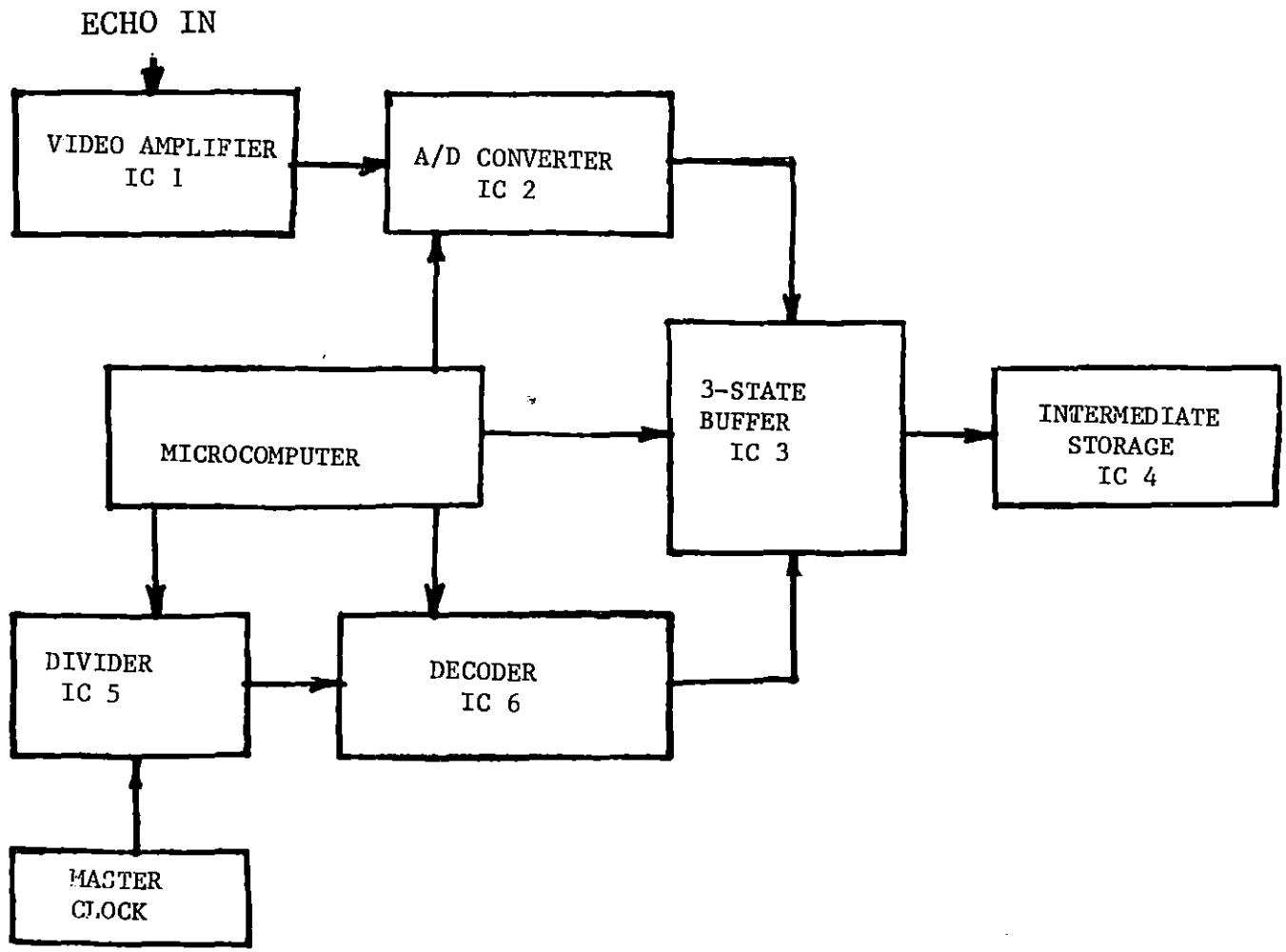
IC 1 LM733 Differential video amplifier

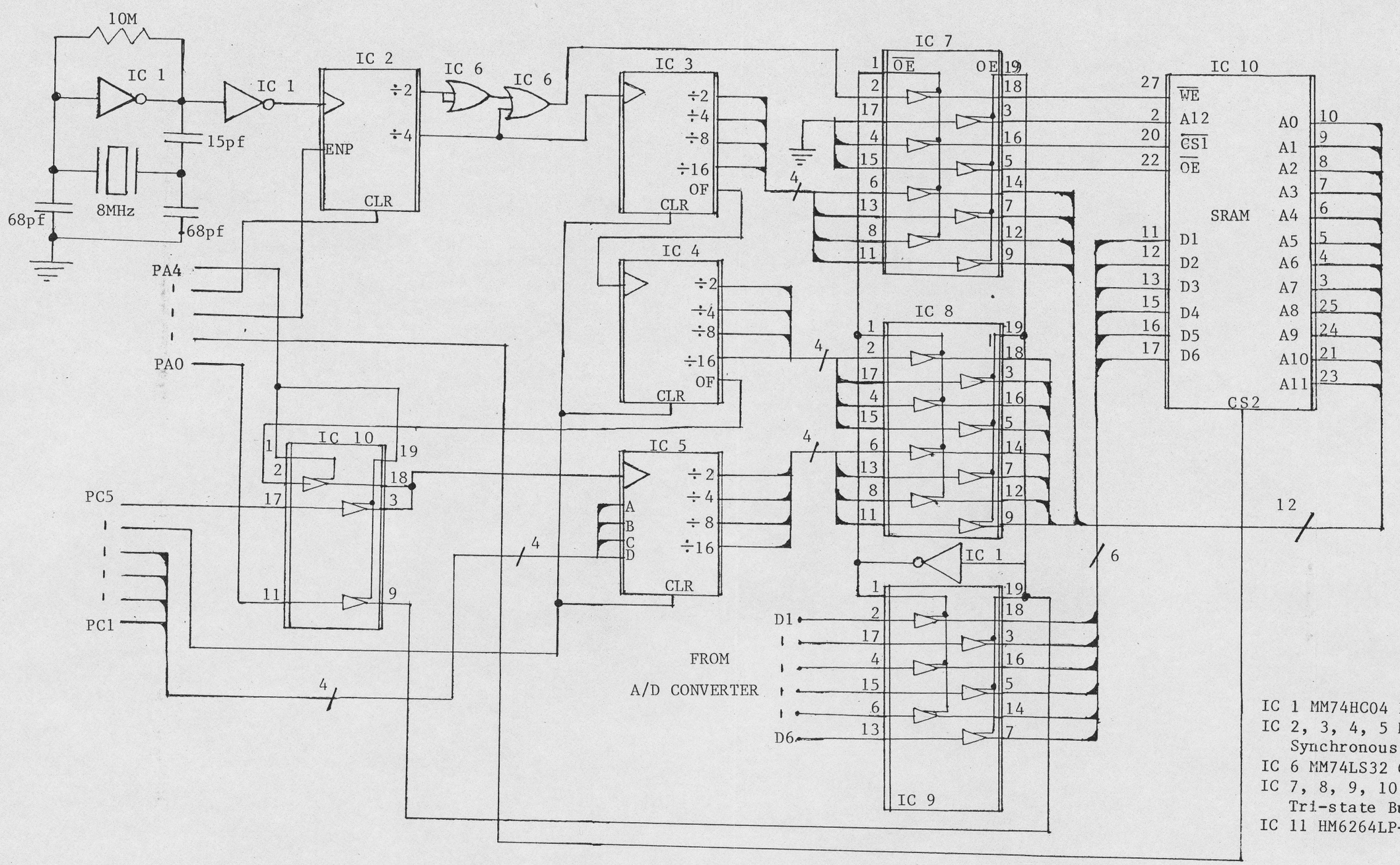
IC 2 CA3300 Flash A/D converter

IC 3 MM74HC241 Octal tristate buffer

IC 4 HM62641p-15 8192 x 8 Static RAM

IC 5, 6 MM74HC161 4-bit Synchronous binary counter


ECHO IN
VIDEO AMPLIFIER
IC 1
A/D CONVERTER
IC 2
MICROCOMPUTER
3-STATE
BUFFER
IC 3
INTERMEDIATE
STORAGE
IC 4
DIVIDER
IC 5
DECODER
IC 6
MASTER
CLOCK



IC 1 MM74HC04 Hex Inverter
IC 2, 3, 4, 5 MM74HC161 4-Bit Synchronous Binary Counter
IC 6 MM74LS32 Quad 2-Input OR Gate
IC 7, 8, 9, 10 MM74HC241 Octal Tri-state Buffer
IC 11 HM6264LP-15 8192 x 8-Bit Static RAM

FIGURE 8. Circuit diagram of the data acquisition interface

acts as a divider and supplies the signals to control the data sampling rate. All address, data and control lines are connected through 74HC241 tristate buffers. The most significant address line, two most significant data lines and CS and OE lines of 6264 were set low through the tri-state buffers. The other address lines of 6264 were derived from the outputs of three 4-bit binary counters (74HC161) connected in cascade. This counter stage is started from the 2 MHz output of the divider. The 6 least significant data lines were derived from the output of the A/D converter. The WR signal was the one used for the clock of the A/D converter. CS2 was controlled by PA1 of the computer parallel I/O port. The timing diagram of the signals at the intermediate memory during data acquisition is shown in the Figure 9. During data acquisition, address, data and control lines from the data acquisition interface to the intermediate storage are enabled and those from the computer are disabled. Now the memory acts as an intermediate or buffer memory. Alternately, when the address, data and control lines from the computer to the memory are enabled and those from the data acquisition interface are disabled, the memory acts as a computer main memory addressable between locations 4000H-5FFFH.

A single 5 volts power supply was used for both the computer board and the data acquisition interface. When the power is turned on, it takes some time for the computer to setup and initialize the input output ports. The address, data and control buses of the computer were directly connected to the data acquisition board. Pin PC0 controls the tristate buffers and the bidirectional switches connected to the computer bus. It is required that these tristate buffers and the bidirectional switches

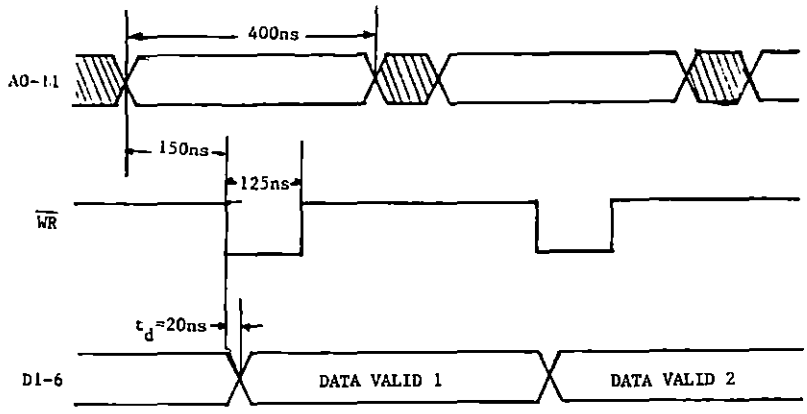
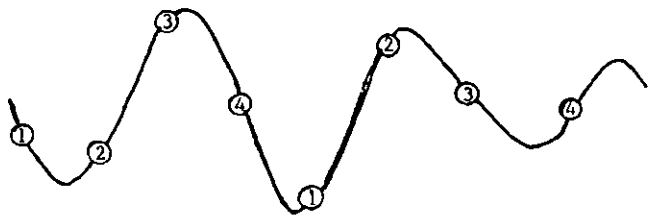


FIGURE 9. Timing diagram of the intermediate storage during the data acquisition

must be in off state condition during the initialization of the computer board. A SPDT switch connected to the ground, PC0 and the control line of the tristate buffers and the bidirectional switches solves this problem. The tristate buffers and the bidirectional switches are disabled using the toggle switch when the system is turned on. After power up control of the tristate buffers and the bidirectional switches is transferred to PC0.

An effective sampling rate of 8 MHz from an actual sampling rate of 2 MHz is achieved by triggering the pulser four times successively, with a delay of 0, 124, 240 and 364ns, respectively. The same sampling procedure was maintained each time. Figure 10 shows the above methodology. After the first sampling procedure, the digitized data were transferred to main memory at location 1000H, 1004H, and so on. After the second sampling procedure, the digitized data were transferred to main memory at



1 Sampled during first pass
2 Sampled during second pass
3 Sampled during third pass
4 Sampled during fourth pass

FIGURE 10. Methodology of the repetitive sequential sampling

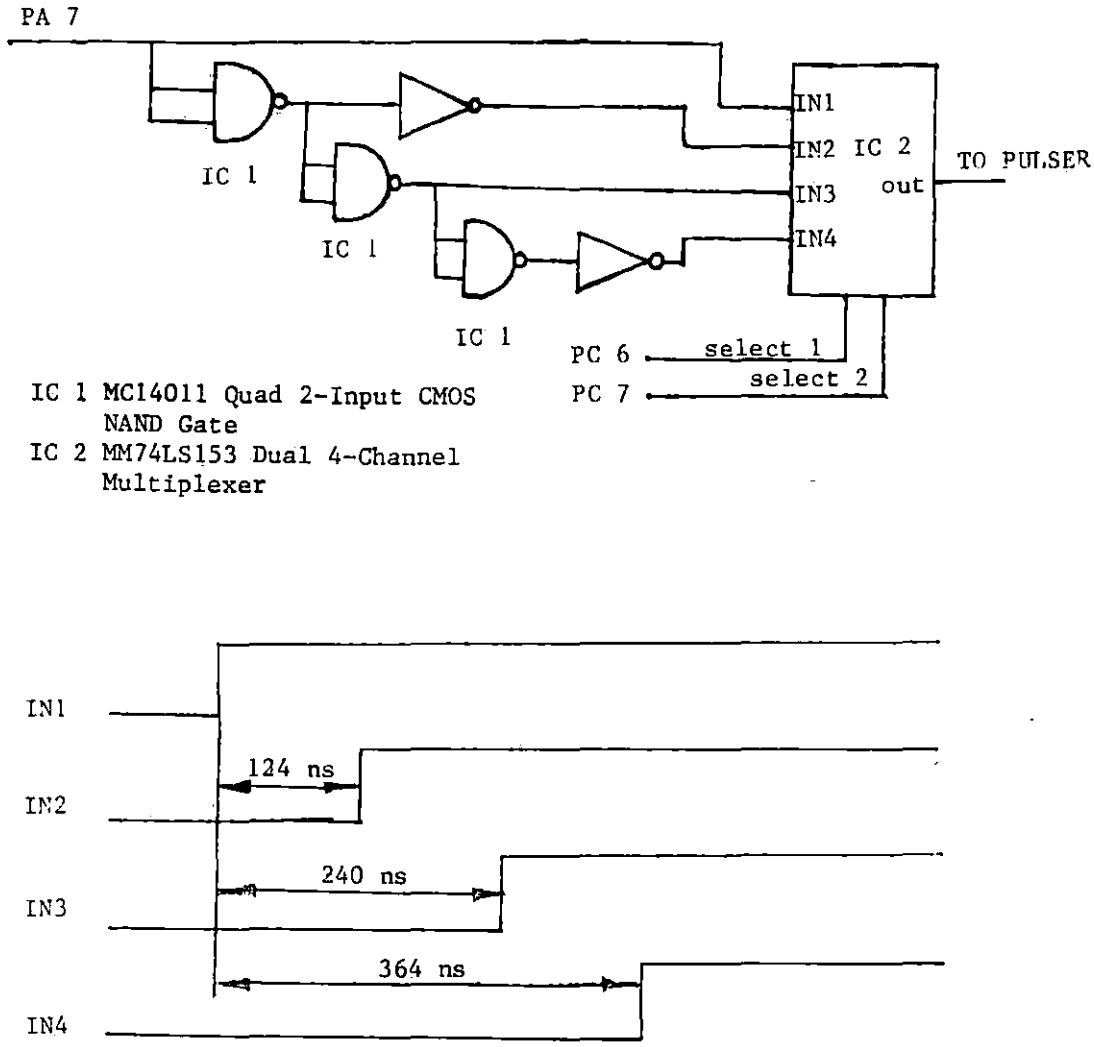


FIGURE 11. Delay-multiplexer circuit and timing diagram

location 1001H, 1005H, and so on. After the third sampling procedure, the digitized data were transferred to main memory at location 1002H, 1006H, and so on. After the fourth sampling procedure, the digitized data were transferred to main memory at location 1003H, 1007H, and so on. Figure 10 shows the methodology of this sampling sequence.

The delay-multiplexer circuit used to achieve repetitive sequential sampling is shown in Figure 11. The delays are achieved by using a slow CMOS NAND gate MC14011. Each gate has a propagation delay of 120 ns. The error introduced by the propagation delay caused by the inverters was neglected. The 4 ns propagation delay of the inverter is very small when compared with that of a MC14011 NAND gate, which is 120 ns. Pin PA7, which triggers the pulser, is connected to the delay circuit as shown in Figure 11. The four outputs of the delay circuit each with a delay of 0, 124, 240 and 364ns are connected to the inputs of the multiplexer (74LS153). Figure 11 shows the delay circuit outputs timing diagram. The computer I/O port pins PC6 and PC7 are connected to the select pins of the multiplexer. So proper input is selected by sending PC6 and PC7 suitable values to PC6 and PC7.

3.6. Digital to Analog Conversion and Display

The stored digital data were converted into an analog signal by the National DAC808. It is an 8-bit digital to analog converter. Figure 12 shows the circuit diagram of the digital to analog conversion circuit. The two least significant input data bits are grounded. Port B was used to send data to the input of DAC808C. The reference Ref+ and Ref- were adjusted for -2.5 Volts and 0 Volts, respectively. This produces an

inverted output voltage. The output of DAC808 can be displayed on an oscilloscope.

3.7. Program and Control

The 8052AH has a BASIC interpreter and supports both BASIC and assembly language. The main program in is written in BASIC. The flow chart of the main BASIC program is shown in Appendix A. The main BASIC program calls assembly language subroutines where precision timing and high speed is necessary. Precision timing is required during sampling and triggering of the pulser. The necessity of high speed execution is required during the transfer of the data from the intermediate storage to the main memory. Initialization of the parallel I/O ports and enabling/disabling the lines where precision timing is not needed is done by BASIC.

A software package purchased from Micromint, Inc. provides an assembler and was used to assemble all assembly language programs.

The main BASIC program listing is shown in Appendix B. The BASIC program first initializes all the three parallel I/O ports as output ports. Port A yields most of the control signals, Port B is dedicated to digital to analog conversion and Port C controls the three counters connected in cascade which generate the address for the intermediate memory and the multiplexer used for the repetitive sequential sampling. An option has been provided where starting address for the acquisition of the data in the intermediate memory can be changed by sending suitable values to PB1, PB2 and PB3. PB1, PB2, and PB3 are connected to the input of three most significant bits of the address generator counter.

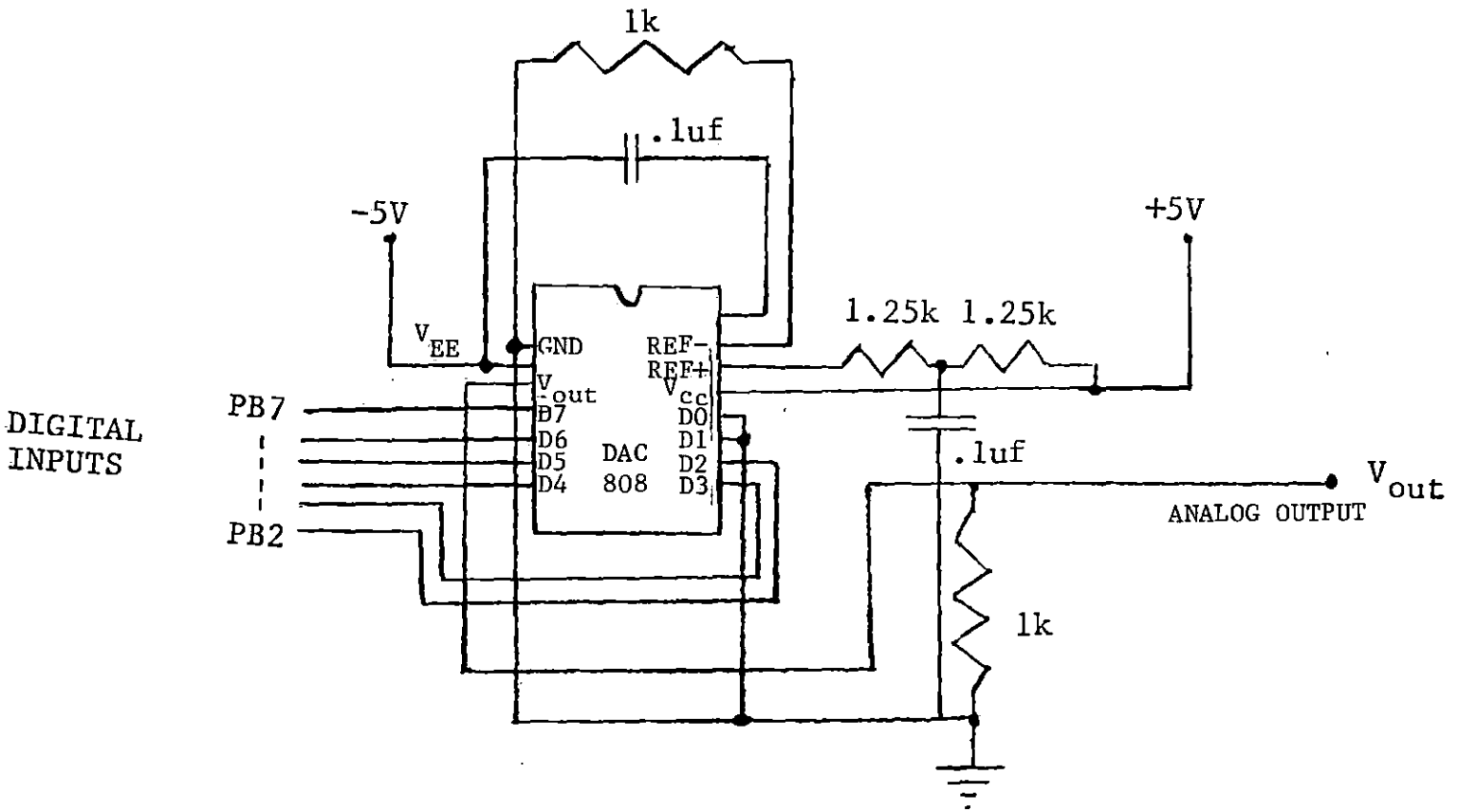


FIGURE 12. D/A conversion

After the initialization of the parallel I/O ports and address generating counters and selecting the proper input in the multiplexer, the main BASIC program calls an assembly language subroutine, Sampler. This assembly language subroutine listing is shown in Appendix C. The address, data and control lines from the data acquisition interface to the memory are enabled and those from the computer were disabled. Memory is enabled and the sampling process was started by enabling the clock generator counter. A trigger pulse from PA7 is sent to the pulser through the delay circuit and the multiplexer. After the required sampling time, the clock generator counter was disabled and subsequently the address, data and control lines are disabled and the program control was returned to the BASIC program.

The next step is to transfer the data into main memory. Address, data and control lines from the computer to the memory are enabled and those from the data acquisition circuit were disabled. Starting address of the main memory for the data storage was provided. Data-Mov, an assembly language subroutine was called to transfer the data. The assembly language program is shown in Appendix D. Now the intermediate memory can be addressable between location 4000H-5FFFH. The sampled data at location 4000H were transferred to location 1000H, data at 4001H were transferred to location 1004H and so on. The above procedure was continued until the required number of samples were transferred and the program control was returned to BASIC.

The same procedure of sampling, triggering and data transferring was repeated four times, and each time suitable input was selected in the multiplexer and the starting address of the main memory during the data

transfer was incremented by one, i.e., 1001 was the starting address during second time and so on.

The stored data in the memory starting location 1000H were converted into an analog signal by the D/A converter. DA-convert, an assembly language subroutine shown in Appendix E was called by the BASIC program. This assembly language subroutine sends the stored data to Port B which is connected to the input of the D/A converter. The analog representation of the stored data can be seen on an oscilloscope connected to the output of the D/A converter. The analog representation of the stored data can also be seen on the computer terminal by a BASIC program shown in Appendix B. Upto 74 locations whose starting address is previously selected in the program can be viewed on the terminal.

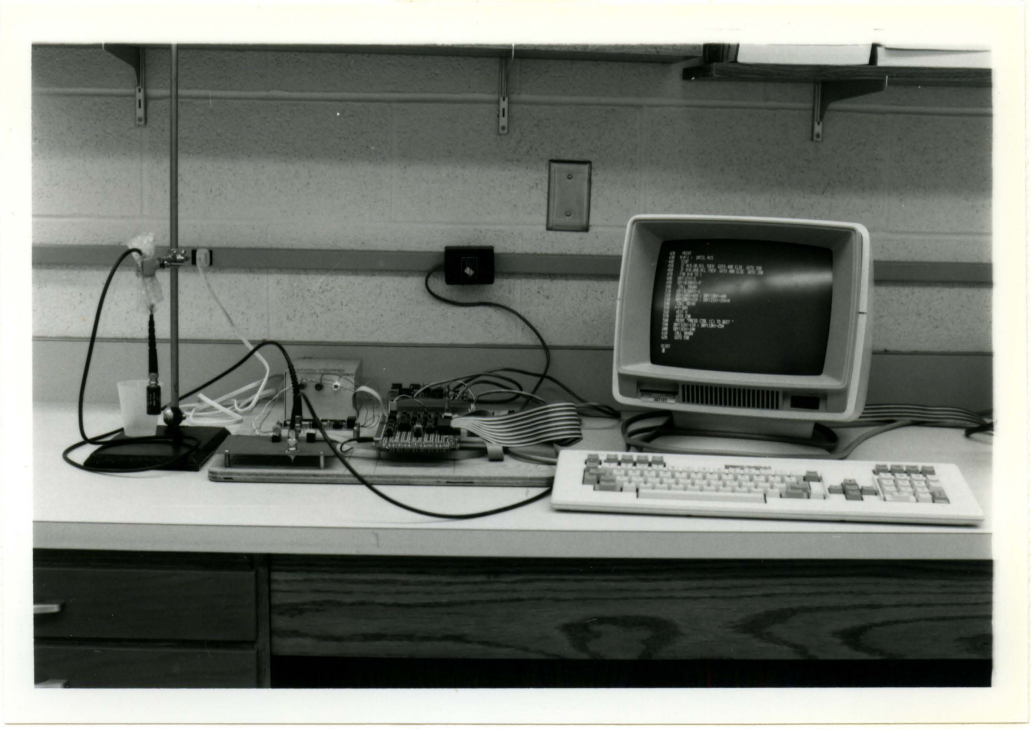
4. RESULTS AND CONCLUSIONS

In sampling the reflected ultrasonic pulse echo signals it is important that the wave shape be preserved. This requires sampling at a higher frequency than the minimum indicated by the Shannon's sampling theorem. For instance, when sampling a sine wave at minimum sampling frequency, i.e., two samples per cycle, the sampling will be error free if the samples happen to be taken at the peaks of the sine wave but the signal will be zero if the samples are taken at zero crossings. The ultrasonic signal generated by the transducer of 2.25 MHz center frequency was sampled at 8 MHz.

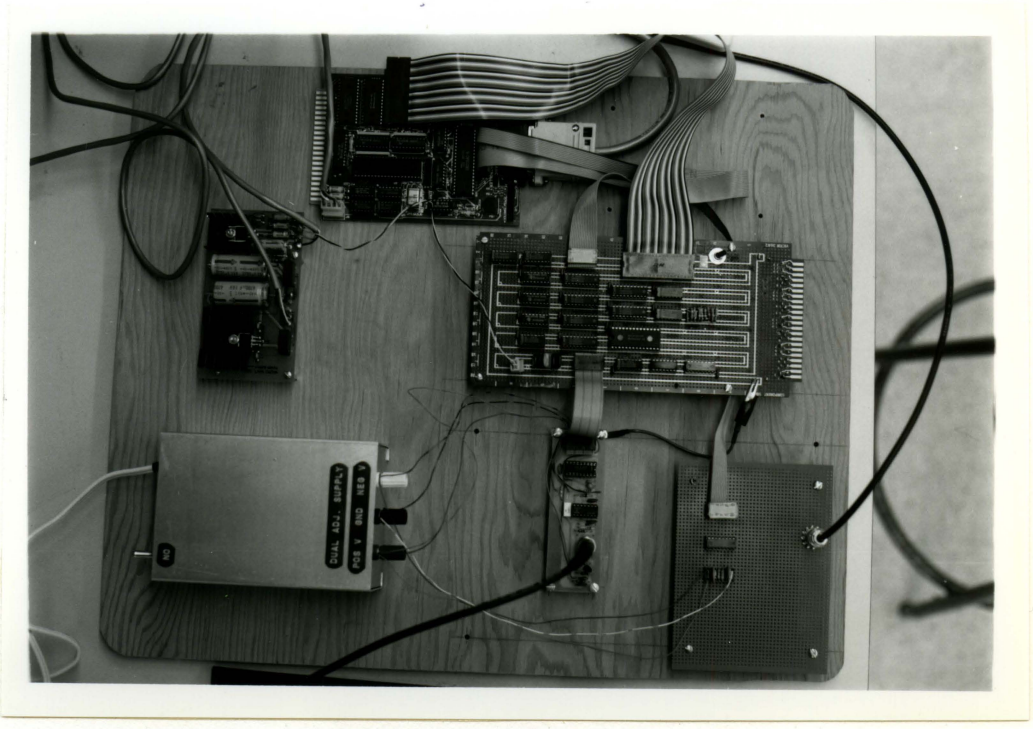
Figure 13(a) shows the photo of the complete system. The pulser, video amplifier A/D converter, data acquisition board, microcomputer and D/A converter were fastened on a board and its photo is shown in Figure 13(b).

The system was tested at many stages. The signal was tested at the output of the pulser to test its performance and shown to perform properly. The magnitude, width, fall time and rise time of the pulse produced by the pulser were measured and are 4.8 V, 240 ns, 8 ns, and 42 ns, respectively.

The LM733 video amplifier was tested, and the amplifier shown to amplify properly. The gain of the LM733 was measured at different frequencies (100 Hz - 10 MHz) and a plot of frequency v/s gain is shown in the Figure 14.



(a)



(b)

FIGURE 13. Photo of the system

CA3300 A/D Flash Converter was tested at different steady state input voltages and shown to convert properly. A plot of the analog input to the digital output measured is shown in Figure 15.

The control signal (shown in Figure 3) for the A/D conversion and to write the data in the intermediate storage was tested for its function. The data acquisition part was tested by sending different steady state voltages to the input of the A/D converter and each time the control signal was sent for one cycle using an assembly language subroutine and the stored data were verified. The system performed properly.

The DAC808 D/A converter was tested for different steady state inputs and shown to convert properly.

Figure 16 shows the photo of the pulse echo signal at the input of the A/D flash converter and Figure 17 shows the plot of the data obtained from the same signal. The magnitude and frequency of the signal is preserved.

The main BASIC program and assembly language subroutines written for the system worked. The options provided during the data sampling are the sampling time, upto 8x255 usecs can be selected and the sampling frequency, either 4 MHz or 8 MHz can be selected. The stored data can be viewed either on an oscilloscope by sending the data into the D/A converter or on the computer terminal, where 70 previously selected locations can be viewed at a time.

The system, which is built to perform sampling, storing and analyzing the ultrasonic pulse echo signal is based entirely on a single chip microcomputer, which is in contrast to most previous work that employed minicomputers and also some mainframe computers. This integral

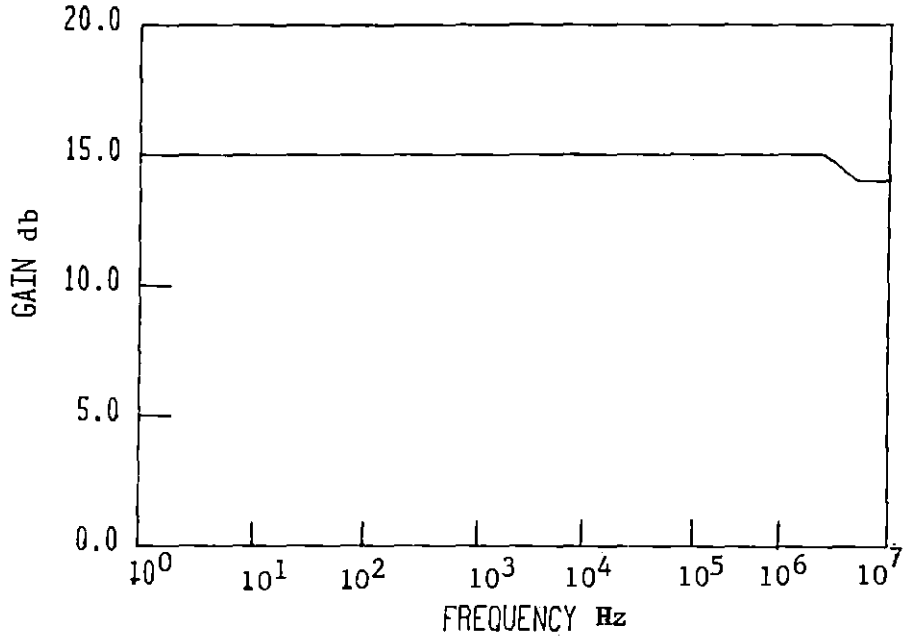


FIGURE 14. Frequency response of the video amplifier

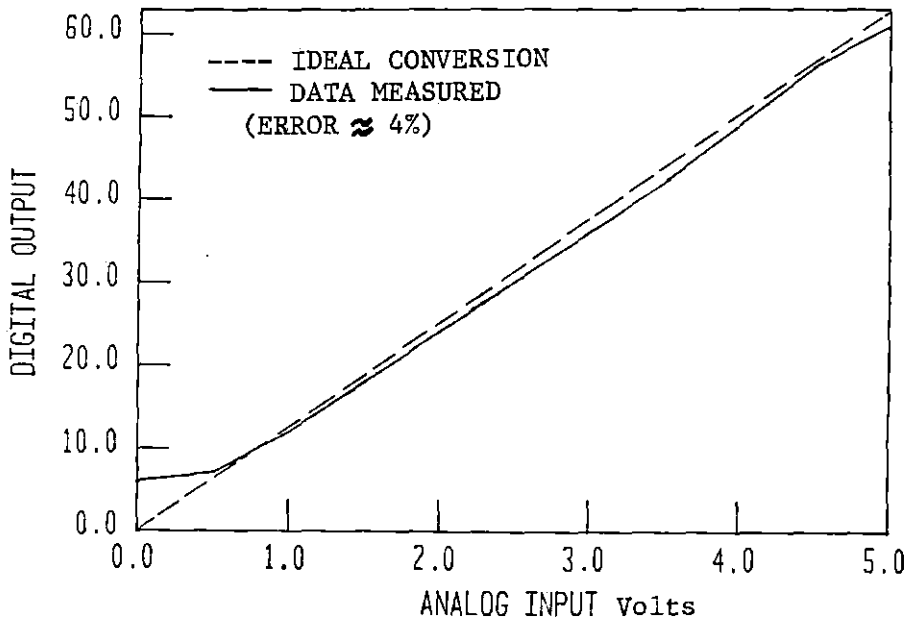


Figure 15. A/D converter output versus input

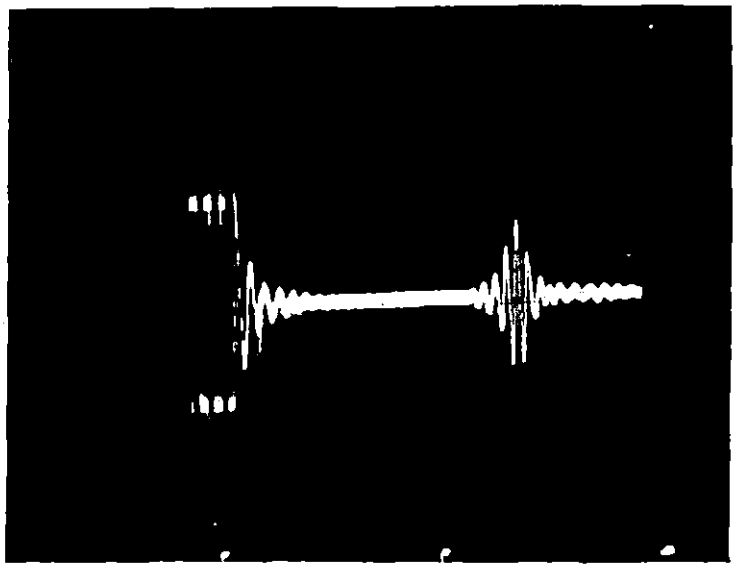


FIGURE 16. Photo of an ultrasonic analog signal

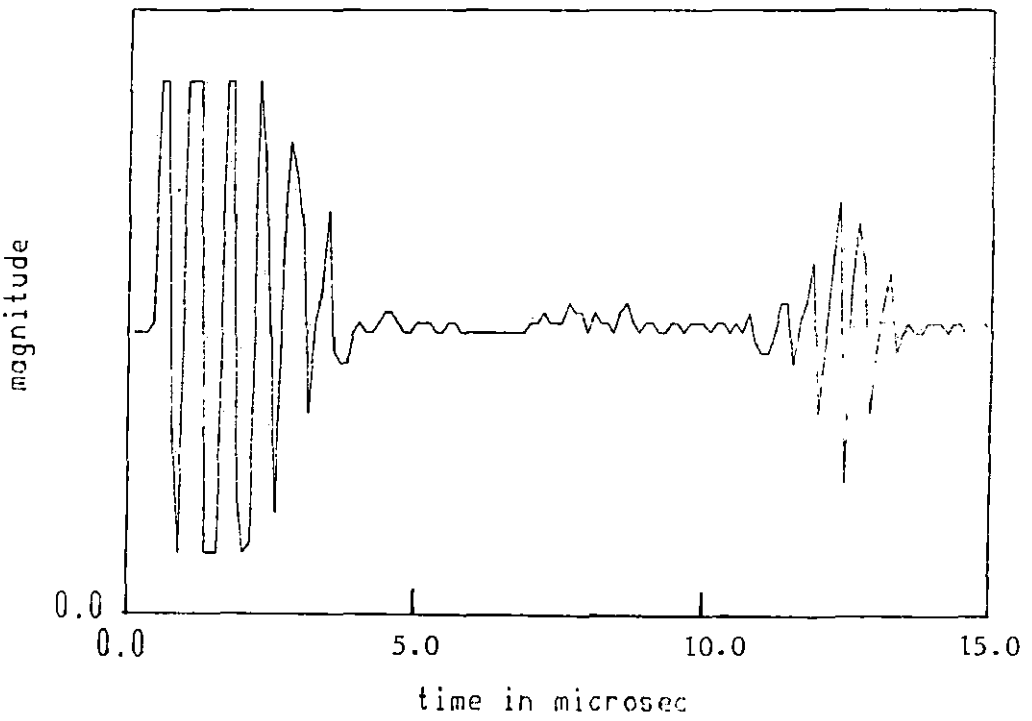


FIGURE 17. A digitized reproduction of the signal shown in Figure 16

ultrasound equipment can process the signal in a real time basis, also any type of biomedical ultrasound signal requiring processing can be solved by this system.

The system is flexible and simple to use. The A-mode ultrasonic data were sampled, stored and digitized and shown to retain the wave shape information.

The sampling speed of the system is limited mainly by the propagation delay of the hardware interface between the intermediate storage and master clock generater. The contributions to the propagation delay are from the three 4-Bit binary address generating counters, each has a maximum propagation delay of 29 ns and from the 3-State buffer which has a maximum propagation delay of 18 ns. The total maximum propagation delay is 105 ns (3x29 + 18 ns). The minimum write cycle time for the intermediate storage (HM6264LP-15) is 150 ns. Hence the minimum write cycle time of the system is 255ns (105 + 150 ns). A maximum actual sampling rate of 4 MHz (1/255ns) can be achieved using this system by changing the clock signal obtained from the master clock generater.

The main problem faced during the fabrication of the system was to minimize the noise in the analog circuits of the system. The received voltage pulse generated by the transducer is in the order of millivolts (0 - 400 mv) and it is susceptible to the noise generated by the surrounding environment. The major contributions to the noise were from the computer board, data acquisition board, the computer terminal and the power supply. To minimize the above mentioned noise, the analog part of the system, consists of the pulser, video amplifier and the A/D converter were built on a separate printed circuit board. This board utilized a

separate power supply. The noise level at the output of the video amplifier was 50 mv, which is very small when compared with the 4V P/P signal. By using the high speed flash A/D converter the necessity of the sample and hold was eliminated.

The center frequency of the transducer used to produce the ultrasonic signal is 2.25 MHz. The magnitude of the signals which are above 4 MHz is small when compared with those of 2.25 MHz signals. The aliasing error produced by the signals of greater than 4 MHz is neglected. This error can be eliminated by using an antialiasing filter connected before the A/D converter.

An improvement to the system includes, building an interface between the system and a large computer, through which the digitized data from the microcomputer can be transferred for any sophisticated signal processing or analysis.

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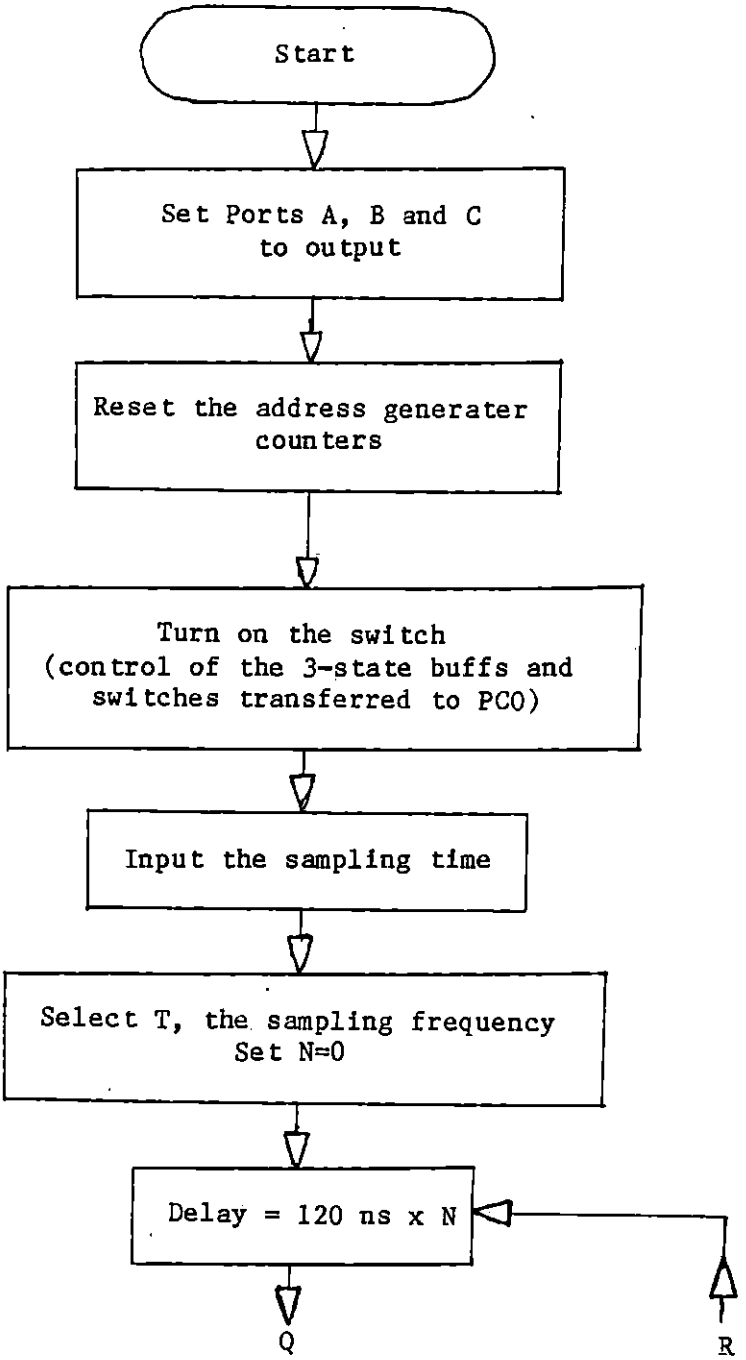
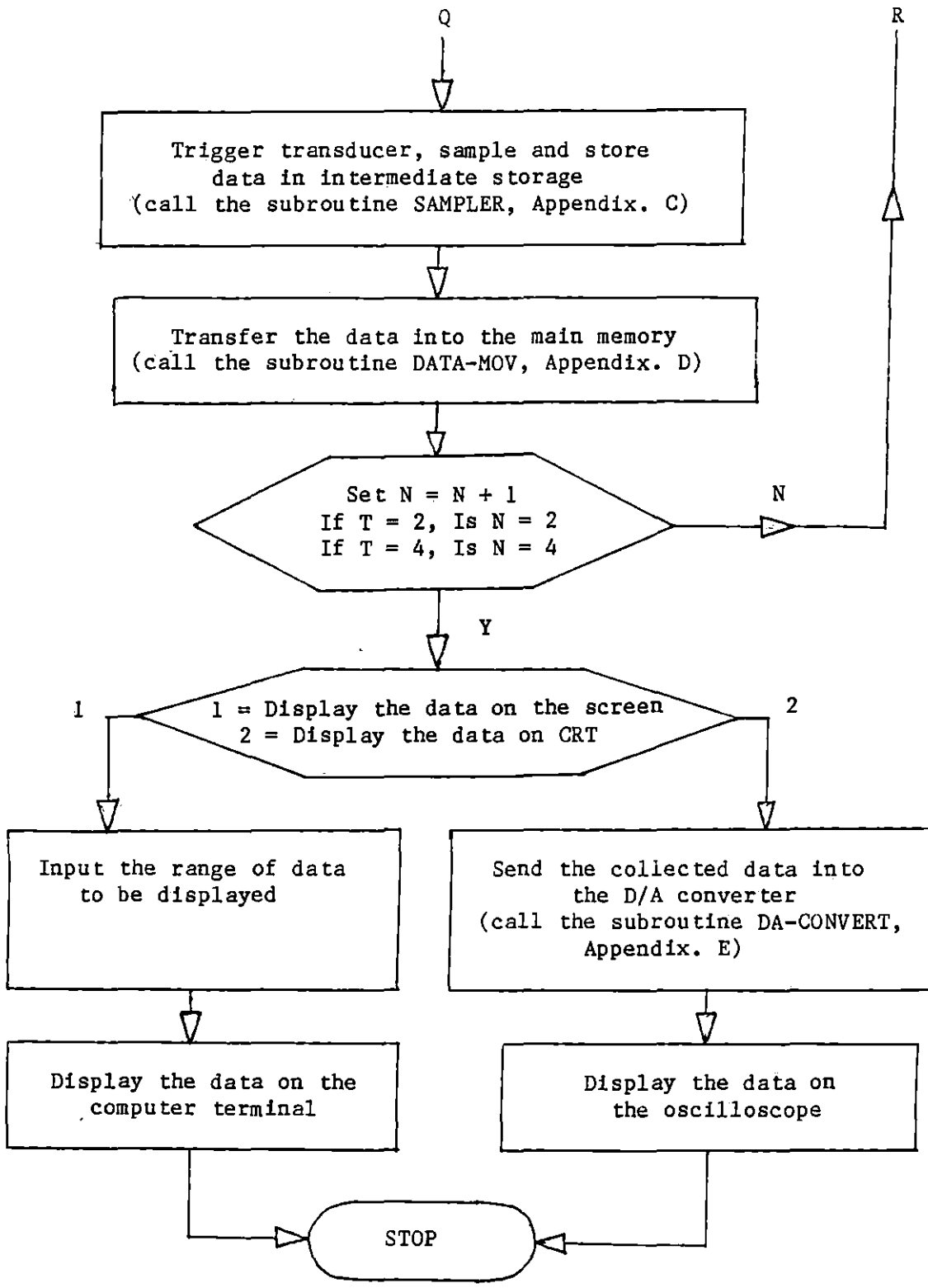
Thanks to my parents and brother, at home for their encouragement and support.

7. APPENDIX A: FLOWCHART OF THE MAIN BASIC PROGRAM




Q
R
Trigger transducer, sample and store data in intermediate storage (call the subroutine SAMPLER, Appendix. C)
Transfer the data into the main memory (call the subroutine DATA-MOV, Appendix. D)
Set N = N + 1
If T = 2, Is N = 2
If T = 4, Is N = 4
N
Y
1 = Display the data on the screen
2 = Display the data on CRT
1
2
Input the range of data to be displayed
Send the collected data into the D/A converter (call the subroutine DA-CONVERT, Appendix. E)
Display the data on the computer terminal
Display the data on the oscilloscope
STOP

8. APPENDIX B: MAIN BASIC PROGRAM

The main BASIC program is stored in the 2764 EPROM provided on the BCC52 computer board. It is the eighth BASIC program in the present EPROM. It can be executed by sending the commands ROM8 <RET> and RUN <RET>.

```
10 STRING 100,10
20 XBY(0C803H)=80H :  REM- INITIALIZE ALL I/O PORTS AS OUTPUT PORTS.
30 XBY(0C802H)=0 :  XBY(0C802H)=20H :  XBY(0C802H)=10H :  REM- RESET
THE ADDRESS GENERATER COUNTERS.
40 S=80H :  REM- SAMPLING TIME = 4 X 80H uSECS.
60 PRINT "SELECT THE SAMPLING RATE"
70 PRINT
80 INPUT "PRESS '4' FOR 4 MHZ OR '8' FOR 8 MHZ....",T
90 PRINT
100 P=0D0H :  REM- MULTIPLEXER SELECTED FOR ZERO DELAY (IN 1)
120 INPUT "TURN ON THE SWITCH AND <RET>",S(0):  REM- SET THE CONTROL
OF THE SWITCHES AND 3-STATE BUFFERS CONNECTED TO THE COMPUTER BUS TO PC0.
130 IF T=4 GOTO 470
140 FOR N=0 TO 3
150 XBY(0C802H)=P :  REM- SELECT RESPECTIVE INPUT IN THE DELAY MU-
TIPLEXER CIRCUIT.
160 DBY(1FH)=S :  REM- REGISTER 1FH HOLDS THE SAMPLING TIME IN
uSEC*4.
```

```
170 CALL 9B60H :  REM- CALL THE SUBROUTINE SAPMLER, APPENDIX B.
180 XBY(0C802H)=1 :  REM- CONNECT THE COMPUTER BUS TO THE INTER-
MEDIATE MEMORY.
190 DBY(20H)=10 :  DBY(21H)=N
200 CALL 9D48H :  REM- CALL THE SUBROUTINE DATA-MOV, APPENDIX C.
210 P=P-40H :  REM- CHANGE THE INPUT SELECTED IN THE DELAY MU-
TIPLEXER CIRCUIT.
220 NEXT N
230 INPUT "PRESS '1' TO DISPAY THE SIGNAL ON THE SCREEN OR '2' TO
DISPLAY IT ON CRT ',D
240 PRINT
250 IF D=2 GOTO 580
260 INPUT "AFTER ...  MICROSECONDS..",X :  REM SELECT THE DATA RANGE
TO BE DISPLAYED.
270 X=X * T
280 M=27 :  NUMBER OF VERTICAL DIVISIONS.
290 DO
300 FOR A= X TO X   74:  REM- 74 HORIZONTAL DIVISIONS.
310 R=XBY(1125HA):  R=R.AND.3FH
320 L=XBY(1126HA):  L=L.AND.3FH
330 R=INT(R/2) :  L=INT(L/2):  REM- RANGE ADJUSTMENT TO DISPLAY ON
THE SCREEN.
335 REM- PROGRAM TO DISPLAY ON THE SCREEN.
340 IF M>R.AND.M>L THEN GOTO 390
```

```
350 IF M<R AND M<L THEN GOTO 390
360 IF M=R GOTO 400
370 IF L<R THEN GOTO 450
380 IF L>R THEN GOTO 460
390 PRINT " ", GOTO 410
400 PRINT ".",
410 NEXT A
420 PRINT
430 M=M-1:  UNTIL M<5
440 STOP
450 IF M<R.OR.M>L THEN GOTO 400 ELSE 390
460 IF M>R.AND.M<L THEN GOTO 400 ELSE 390
470 FOR N=0 TO 1
480 DBY(1FH)=S
490 XBY(0C802H)=P
500 CALL 9B60H
510 XBY(0C802H)=1
520 DBY(1AH)=41H:  DBY(1BH)=44H
530 DBY(20H)=11H:  DBY(21H)=25HN
540 CALL 9D74H :  REM- SUBROUTINE TO TRANSFER THE DATA SAMPLED AT 4
MHZ.
550 P=P-80H
560 NEXT N
570 GOTO 230
```

```
580 PRINT "PRESS CTRL <C> TO QUIT "
590 DBY(1CH)=11H:  DBY(1DH)=25H
600 DBY(1EH)=1AH
610 CALL 9D9DH:  REM- CALL THE SUBROUTINE DA-CONVERT, APPENDIX D.
620 GOTO 590
```

9. APPENDIX C: SAMPLER, AN ASSEMBLY LANGUAGE SUBROUTINE TO TRIGGER THE PULSER AND STORE THE DATA IN THE INTERMEDIATE STORAGE

The following assembly language subroutine is stored in the EPROM starting at location 9B60H and it has a length of 36 bytes. The register 1FH holds the sampling time * 4 in microseconds provided from the main BASIC program (line 40).

```
;*************************************************************
;
register 1FH holds the sampling time in uSec*4.
;
;*************************************************************
MOV DPTR,0C800H ;load the data pointer with port A address.
MOV A, 1BH ;enable the memory and tristate buffers connected-
MOVX @DPTR,A ;to the data acquisition lines and the memory.
MOV A, 1FH ;enable clock counter, and start the data storage.
MOVX @DPTR,A
MOV A, 9FH ;trigger the pulser.
MOVX @DPTR,A
MOV A, 1FH
MOVX @DPTR,A
MOV R1,1FH ;load to R1 the sampling time/4 from register 1FH.
BACK2:  DJNZ R2,BACK1 ;check for end of sampling time.
```

```
MOV A, 17H ;disable the clock counter.
MOVX @DPTR,A
MOV A, 12H ;disable the memory.
MOVX @DPTR,A
MOV A, 0 ;disable the tristate buffers.
MOVX @DPTR,A
RET ;return to main BASIC program.
BACK1:  LJMP BACK2
```

10. APPENDIX D: DATA-MOV, AN ASSEMBLY LANGUAGE SUBROUTINE TO TRANSFER THE DATA FROM THE INTERMEDIATE STORAGE TO THE MAIN MEMORY

The following assembly language subroutine is stored in the EPROM starting at location 9D48H and it has a length of 41 bytes. This program was used to transfer the data from the intermediate storage to the main memory to achieve an 8 MHz sampling rate.

```
;*************************************************************
;
;registers 1AH and 1BH hold the starting address
;of the source and registers 20H and 21H hold the
;starting address of the destination.
;
;*************************************************************
BACK2:  MOV DPH,1AH ;load the data pointer with the starting-
MOV DPL,1BH ;address of the source.
MOV A,@DPTR
INC DPTR
MOV 1AH,DPH
MOV 1BH,DPL
MOV DPH,20H ;load the data pointer with the starting-
MOV DPL,21H ;address of the destination.
MOVX @DPTR,A
INC DPTR
```

```
INC DPTR
INC DPTR ;the next destination address is incremented-
INC DPTR ;four times.
MOV 20H,DPH
MOV 21H,DPL
MOV A, 4AH ;4AH- the two most significant bytes of the-
;ending of the source address.
CLR C
SUBB A,1AH
JNC BACK1 ;check for the end of the transfer.
RET ;return to the main BASIC program.
BACK1:  LJMP BACK2
```

11. APPENDIX E: DA-CONVERT, AN ASSEMBLY LANGUAGE SUBROUTINE TO SEND THE DATA TO D/A CONVERTER

This assembly language subroutine is stored in the EPROM starting at location 9D9DH and it has a length of 29 bytes.

```
;*****************************************************************
;
;registers 1CH and 1DH hold starting address of
;the data for the anlog conversion.
;register 1EH holds two most significant bytes of
;the address upto which the conversion is done.
;
;*****************************************************************
BACK2:  MOV DPH,1CH ;load the starting address in the-
MOV DPL,10H ;data pointer.
MOVX A,@DPTR
INC DPTR
MOV 1CH,DPH
MOV 10H,DPL
MOV DPTR,0C801H ;send the data to PORT B which is
MOVX @DPTR,A ;connected to the D/A converter.
MOV A,1EH
CLR C
SUBB A,1CH ;check if conversion is done.
```

```
JNC BACK1
RET ;return to main BASIC program.
BACK1:  LJMP BACK2
```