A PDP-8/E digital interface for the Heath H10 paper tape reader/punch

by

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TABLE OF SYMBOLS

ABSLDR	Absolute Loader
AC	Accumulator
BCD	Binary Coded Decimal
BUILD	System generation program for OS/8
CO	OMNIBUS signal[1]
C1	OMNIBUS signal[1]
CPU AC	Central Processing Unit Accumulator
DATA	Data Bus data line (OMNIBUS signal)[1]
H	Active high
IC	Integrated circuit
INTERNAL I/O	OMNIBUS signal[1]
I/O	Input/Output
IOP	Input/Output pulse
I/O PAUSE	OMNIBUS signal[1]
IOT	Input/Output transfer
L	Active low
MD	Memory data line (OMNIBUS signal)[1]
PIP	Perpheral Interchange Program
RDR	Reader
SKIP	OMNIBUS signal[1]
TP 3	Timing pulse 3 (OMNIBUS signal)[1]
	Represents an OMNIBUS signal

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[1] For all OMNIBUS signals, refer to the APPENDIX.

INTRODUCTION

Twelve-bit minicomputers such as the Digital Equipment Corportation (DEC) PDP-8/E (1) or equivalent are often used in biomedical experimentation and research by hospitals and clinics to control and monitor biological and physiological parameters. To maintain their versatility, minicomputers are commonly used in conjunction with other peripherals and memory devices to perform the basic task of inputting programs and outputting information. Although the cost of minicomputers and their peripherals has decreased considerably in the past few years, to purchase a complete computer system, one would have to spend anywhere between ten to twenty thousand dollars or more depending on the quality and the complexity of the system.

In an effort to minimize this cost, a study was undertaken to develop a more effective method of accomplishing the task of information input/output. This study utilizes the DEC PDP-8/E minicomputer; therefore, all discussions following refer to this sytem, although applications to other equivalent mini and micro computers are possible. There are several means of inputting and outputting information. The most common of these are the Teletype, DECwriter (LA36), DEC high-speed paper tape reader/punch, Floppy disk memory system and DECtape transport. However, there are advantages and disadvantages associated with each one of these to be considered.

To further elaborate on the various methods of information input/output listed above, consider the following example. Suppose a program is entered into the computer by keying it in via the front panel switches

of the PDP-8/E and it is run and the desired output is obtained. It is then decided to save this program. What are the methods available which allow you to save this program? The exotic methods, of course, are such things as DECtape or Floppy disc which are moderately expensive at present (DECtape costs around $4000, Floppy disc around $2500) and in terms of relative cost, most people cannot afford them. The next choice to consider may be the Teletype. It is true that the Teletype with proper interfacing is capable of reading information into the PDP-8/E memory and can save information on paper tape. However, there are some disadvantages in using the Teletype:

1) Teletypes are expensive (around $1300).

2) Teletypes are mechanical, subject to wear problems.

3) Teletypes are slow (operate at a data rate of 110 baud).

One might consider the DECwriter (LA36); this unit has several advantages over the Teletype. The DECwriter has a lower failure rate than the Teletype and is similar in cost but three times as fast. Although not directly related, another feature of the DECwriter is its ability to communicate back and forth at 300 baud over fairly long lines, thus making it about as fast a device as one can get that is versatile. Since the ultimate goal is to input and output information as fast as possible and yet not go overboard on price, the DECwriter seems like the ideal device. Unfortunately, the DECwriter unlike the Teletype, has no paper tape input/output capability. Thus if you have only a DECwriter and a PDP-8/E, you have no method of programming the PDP-8/E with paper-tape programs or saving programs (other than a hard copy that the DECwriter provides). Therefore to maintain the DECwriter's speed and yet eliminate

the tedious task of entering programs step by step, the objective becomes one of obtaining paper tape capability at low cost.

Since paper tape reader/punch units are expensive, time was spent researching the capabilities and costs of different units. The Heath model H10 paper tape reader/punch was found to be the most cost effective unit available at the present time. It can read at a speed of 50 characters per second and can punch at a speed of 10 characters per second using 8-level, 1 inch paper tape. It costs $500 as opposed to a $5000 DEC unit, thus possessing an economic avdantage. the DECwriter in conjunction with this Heath reader/punch constitutes a fast and inexpensive system which has the ability to read information into the PDP-8/E and transfer information from the PDP-8/E to the inexpensive medium of paper tape.

One might argue that with the presence of Floppy disc, DECtape, and magnetic tape on the market, paper tape is a little bit on the obsolete side. But there are some good reasons to justify the use of the paper tape. One of the advantages of paper tape is that it has a relatively long life. Better yet, if you put the information on mylar tape as opposed to paper, it will last virtually forever.

Another advantage is that paper tape has a built-in method of troubleshooting. For example, if you were to punch a program on paper tape and then read it back in the computer and it didn't work, you could actually read down through that paper tape and find out where the error had occurred. If there were no errors and the information was still not being received at the computer, then you could automatically say the problem is within the reader. The above method of troubleshooting is not applicable to other

input/output units such as magnetic tape recorders. To find out whether the recording on a magnetic tape is correct is a fairly difficult operation.

Other advantages of paper tape are that heat, cold, or magnetic fields won't affect it. Also, the problem of crosstalk developed on magnetic tapes after long periods of storage is eliminated when using paper tapes.

It should be mentioned that, like other mechanical units, there are mechanical disadvantages associated with the memory units utilizing paper tape. Other disadvantages associated with paper tape are that it is slow and limited in its density of recording. In most applications, however, you can fit all of the information for a substantial program on a small roll of paper tape. So paper tape, although slow and having lower density capability than many of the newer techniques, still has a very valid place in programming and storing information.

The Heath paper tape reader/punch unit, as supplied, has to be interfaced to the PDP-8/E minicomputer in such a way that the action of the reader and punch can be controlled from program instructions (2). This task involves both hardware and software aspects of interfacing. In the hardware design of the interface various fundamental points such as the device address selection, operations decoding, input/output to the bus, and flags and their conditions have to be considered. For the software aspect of the interface, one has to worry about the coding of a device handler program in order to actually control the action of the Heath reader/punch with the program instruction (3).

It is the objective of this research to interface the Heath reader/

punch to the DEC PDP-8/E minicomputer, thereby developing an economical method of information input/output and storage for use in biomedical experimentation and research. Although the details of this interfacing would vary with other equivalent minicomputers, the principles involved remain very similar.

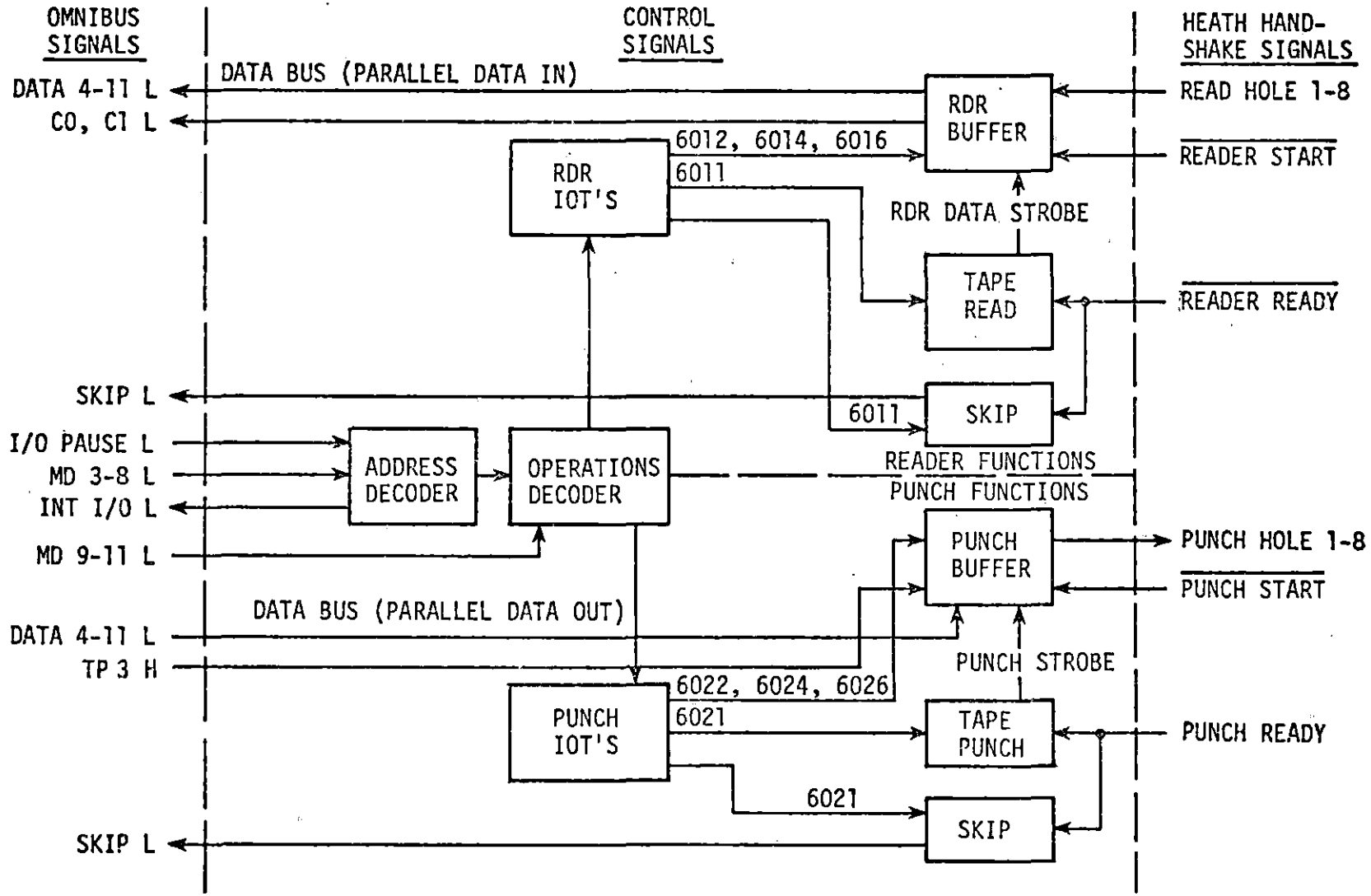
HEATH CONTROL INTERFACE FUNCTIONAL DESCRIPTION

A block diagram of the Heath control interface is illustrated in Figure 1. The primary logic/functions needed to interface the Heath unit to a PDP-8/E are illustrated by blocks. The ADDRESS DECODER provides selection logic to ensure that the processor is communicating with the Heath unit rather than some other device. It receives memory data (MD 3 - MD 8), decodes them, and signals the OPERATIONS DECODER that this input/output transfer (IOT) instruction is addressed to the unit. The input/output (I/O) PAUSE signal is used as a gating input to ensure that the instruction is an IOT instruction. If MD 3 to MD 8 equal 01(octal), the reader is addressed and 02(octal) addresses the punch (4).

The OPERATIONS DECODER begins to function when the ADDRESS DECODER signals that the reader or punch has been addressed. The OPERATIONS DECODER then looks at bits MD 9 to MD 11 and decodes the type of instruction to be performed (4). The OPERATIONS DECODER is divided into two sections, reader and punch functions. Only one function can be turned on during any one IOT. After the function has been selected, the OPERATIONS DECODER enables all of the other functional blocks. If the Heath unit control is to read information, the OPERATIONS DECODER enables the Heath unit TAPE READ and READER BUFFER. If the Heath unit control is to punch information, the OPERATIONS DECODER enables the Heath unit TAPE PUNCH and PUNCH BUFFER.

The reader function is represented by the logic blocks above the broken line in Figure 1. Three IOT instructions 6012 (Read Reader Buffer Register), 6014 (Fetch Reader Character) and 6016 (Read Buffer, Fetch

Figure 1. Interface control board block diagram


OMNIBUS SIGNALS
CONTROL SIGNALS
HEATH HAND-SHAKE SIGNALS
DATA 4-11 L
CO, C1 L
DATA BUS (PARALLEL DATA IN)
RDR BUFFER
READ HOLE 1-8
READER START
6012, 6014, 6016
6011
RDR IOT'S
RDR DATA STROBE
TAPE READ
READER READY
SKIP L
6011
SKIP
I/O PAUSE L
MD 3-8 L
INT I/O L
MD 9-11 L
ADDRESS DECODER
OPERATIONS DECODER
READER FUNCTIONS
PUNCH FUNCTIONS
PUNCH BUFFER
PUNCH HOLE 1-8
PUNCH START
DATA BUS (PARALLEL DATA OUT)
DATA 4-11 L
TP 3 H
PUNCH STROBE
6022, 6024, 6026
6021
PUNCH IOT'S
TAPE PUNCH
PUNCH READY
6021
SKIP
SKIP L

Reader Character), read the information currently over the photo array and then initiate tape feed. When either of these instructions is decoded by the OPERATIONS DECODER logic, the TAPE READ logic generates a READER (RDR) DATA STROBE pulse which enables the READER (RDR) BUFFER gates and allows the information present on the READ HOLE 1-8 lines to pass through. The 6011 instruction (Skip On Reader Flag) senses the state of the $\overline{\text{READER READY}}$ line. The $\overline{\text{READER READY}}$ line being low, indicates that the information is ready to be transferred. Data on READ HOLE 1-8 lines are transferred to the Central Processing Unit Accumulator (CPU AC) Register by either of the 6012 or 6014 instructions or a microprogram of them both, which is the 6016 instruction.

The punch function is represented by the logic blocks below the broken line in Figure 1. Upon decoding a 602X instruction, the OPERATIONS DECODER logic signals the loading of the information of the DATA BUS 4-11 lines into the PUNCH BUFFER register. At TIME PULSE (TP 3) of the instruction, the PUNCH STROBE signal causes the transfer of the character signals from the PUNCH BUFFER to the PUNCH HOLE 1-8 lines. The 6021 instruction senses the state of the PUNCH READY line. The PUNCH READY lines being high indicates that the punch is ready.

DETAILED LOGIC

The overall schematic diagram of the Heath/PDP-8/E interface is shown in Figure 2. The following subsections discuss in detail the different circuits utilized in the interface. Figures 1 and 2 illustrating the block and the schematic diagrams of the interface, should be referred to when reading these subsections. In all of the diagrams throughout, the symbol ◯— represents an OMNIBUS signal. Letters to the right of each signal name specify the pin assignments of the OMNIBUS and are described in the APPENDIX. The L and H after the signal name identify the most common assertion level. The interface supply voltage (Vcc) is 5 volts. The numbers and descriptions of IC's used are listed in Table 1.

ADDRESS DECODER Logic

The ADDRESS DECODER logic (Figure 3) decodes MD 3 through MD 11. The device address is contained in bits 3 through 8, and the operation code is contained in bits 9 through 11. If the middle six bits are decoded as 01(octal), the OPERATIONS DECODER is directed to the reader functions. If the middle six bits are decoded as 02(octal), the OPERATIONS DECODER is directed to the punch functions. The I/O PAUSE gates the address bits through the decoder. The output of the ADDRESS DECODER logic provides an enabling signal either to the reader or to the punch portion of the OPERATIONS DECODER. It also generates the INTERNAL I/O signal, which is used in the positive I/O Bus Interface to prevent the generation of input/output pulses (IOP's) (4).

Figure 2. Schematic diagram of the Heath/PDP-8/E interface

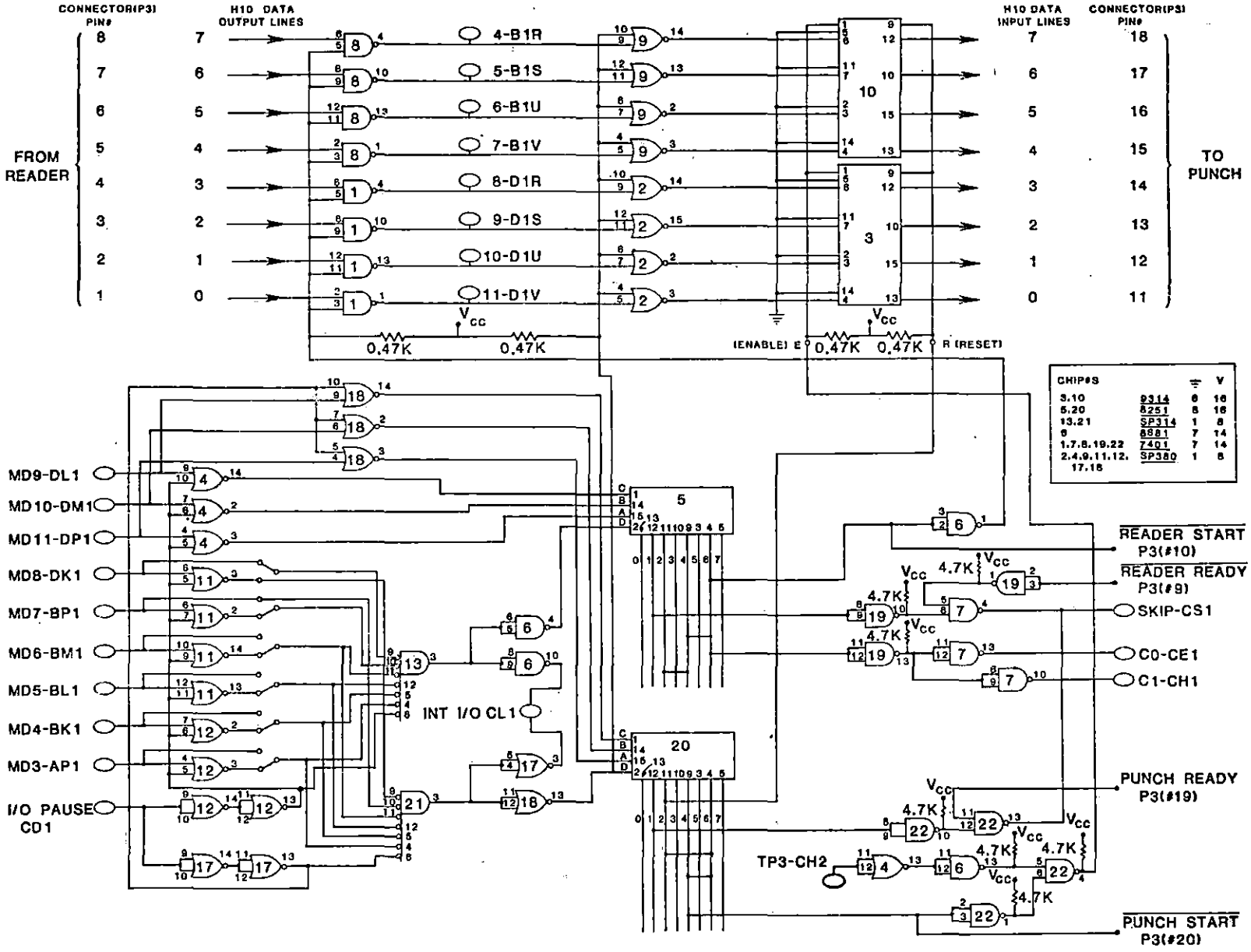

CONNECTOR(P3) PIN#
H10 DATA OUTPUT LINES
FROM READER
8 7
7 6
6 5
5 4
4 3
3 2
2 1
1 0
4-B1R
5-B1S
6-B1U
7-B1V
8-D1R
9-D1S
10-D1U
11-D1V
Vcc
0.47K
0.47K
10
3
(ENABLE) E
R (RESET)
H10 DATA INPUT LINES
CONNECTOR(P3) PIN#
7 18
6 17
5 16
4 15
3 14
2 13
1 12
0 11
TO PUNCH
CHIP#S
3.10 9314 8 16
5.20 8251 5 16
13.21 SP314 1 8
9 8881 7 14
1.7.8.19.22 7401 7 14
2.4.9.11.12. 17.18 SP380 1 8
MD9-DL1
MD10-DM1
MD11-DP1
MD8-DK1
MD7-BP1
MD6-BM1
MD5-BL1
MD4-BK1
MD3-AP1
I/O PAUSE C01
INT I/O CL1
TP3-CH2
4.7K
READER START P3(#10)
READER READY P3(#9)
SKIP-CS1
C0-CE1
C1-CH1
PUNCH READY P3(#19)
PUNCH START P3(#20)

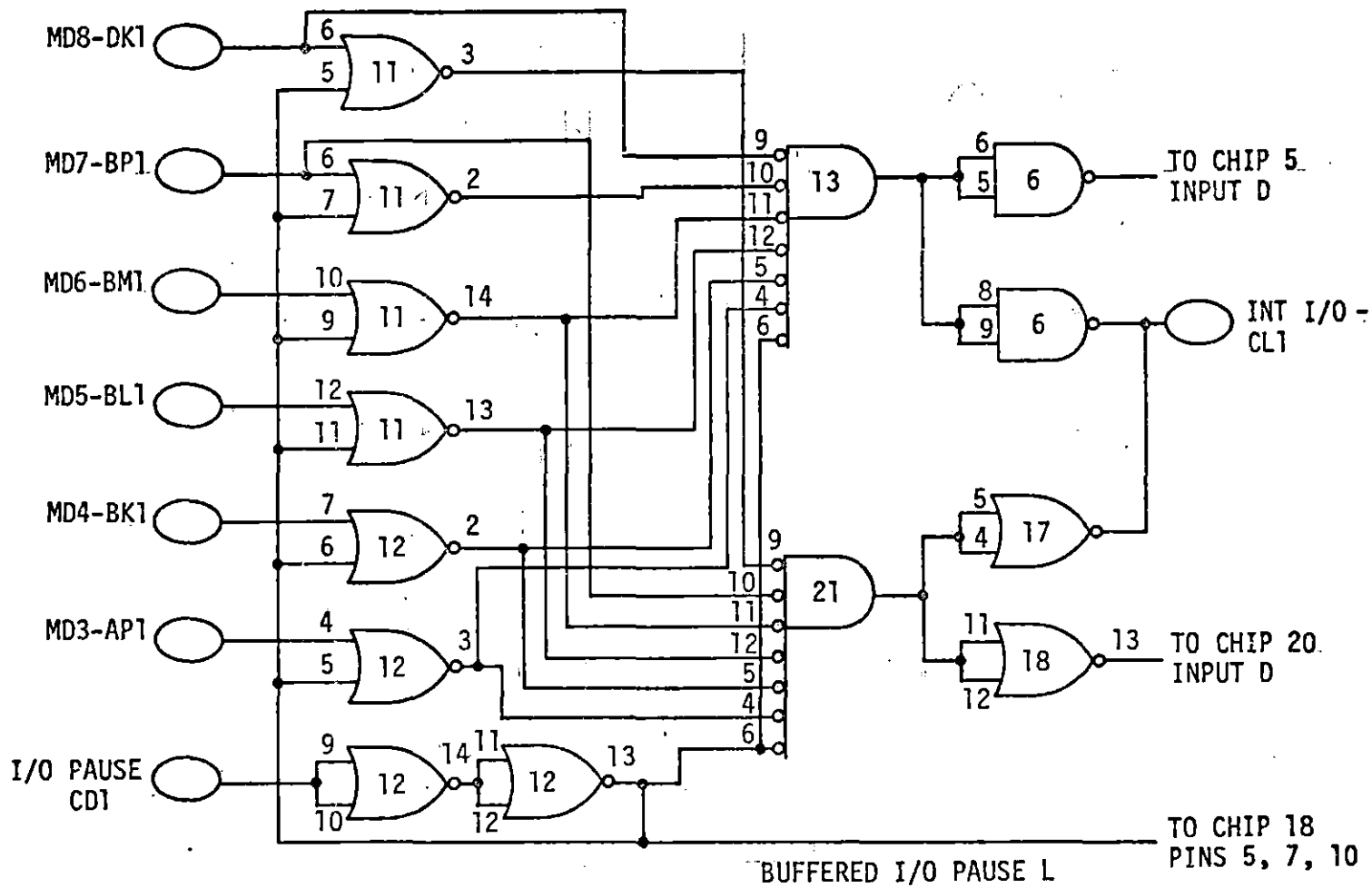
Table 1

MANUFACTURER NUMBERS AND DESCRIPTIONS OF THE IC'S USED[a]

IC CHIP #'s	MANUFACTURER'S TYPE #	FUNCTION
3, 10	9314	Quad Latch
5, 20	8251	BCD-TO-Decimal Decoder
13, 21	SP314	Single 7-input NOR Gate
6	8881	Quad 2-input NAND Gate (with open-collector output)
1, 7, 8, 19, 22	7401	Quad 2-input NAND Gate (with open-collector output)
2,4,9,11, 12,17,18	SP380	Quad 2-input NOR Gate

[a]Note: All IC's are of plastic DIP package type.

Figure 3. ADDRESS DECODER logic diagram


MD8-DK1
MD7-BP1
MD6-BM1
MD5-BL1
MD4-BK1
MD3-AP1
I/O PAUSE CD1
11
12
13
21
6
17
18
TO CHIP 5 INPUT D
INT I/O - CL1
TO CHIP 20 INPUT D
TO CHIP 18 PINS 5, 7, 10
BUFFERED I/O PAUSE L

OPERATIONS DECODER Logic

Figure 4 shows the OPERATIONS DECODER logic. Table 2 lists the high-speed paper tape reader/punch IOT instructions and a description of each (5). The OPERATIONS DECODER logic receives either 01 or 02(octal) from the ADDRESS DECODER logic to enable the reader or punch logic, respectively (4). The operation to be performed is determined by the last three MD bits, MD 9-11. The 601X signal and bits MD 9-11 are applied to the Binary Coded Decimal (BCD)-to-Decimal decoder, (chip #5). This decoder provides the reader IOT signals, as illustrated in Figure 4. The 602X signal and bits MD 9-11 are applied to another BCD-to-Decimal decoder (chip #20), which provides the punch IOT signals.

TAPE READ and SKIP Logic

The TAPE READ and SKIP logic is shown in Figure 5. The TAPE READ logic generates timing signals in response to the IOT instructions 6012, 6014 and 6016. When an IOT instruction (6014, for example) is decoded, the control logic first causes the character to pass through the READER BUFFER gates by the RDR DATA STROBE signal. It then generates stepping signals that cause the reader motor to run. The 6014 signal advances the tape one character by applying a TTL high-to-low transition to the $\overline{\text{READER START}}$ line. 6011 instruction (Skip on Reader Flag) senses the state of the $\overline{\text{READER READY}}$ line in the SKIP logic. The $\overline{\text{READER READY}}$ line being low indicates that the data are ready to be transferred. When this line is low, the program counter is incremented so that the next sequential instruction is skipped.

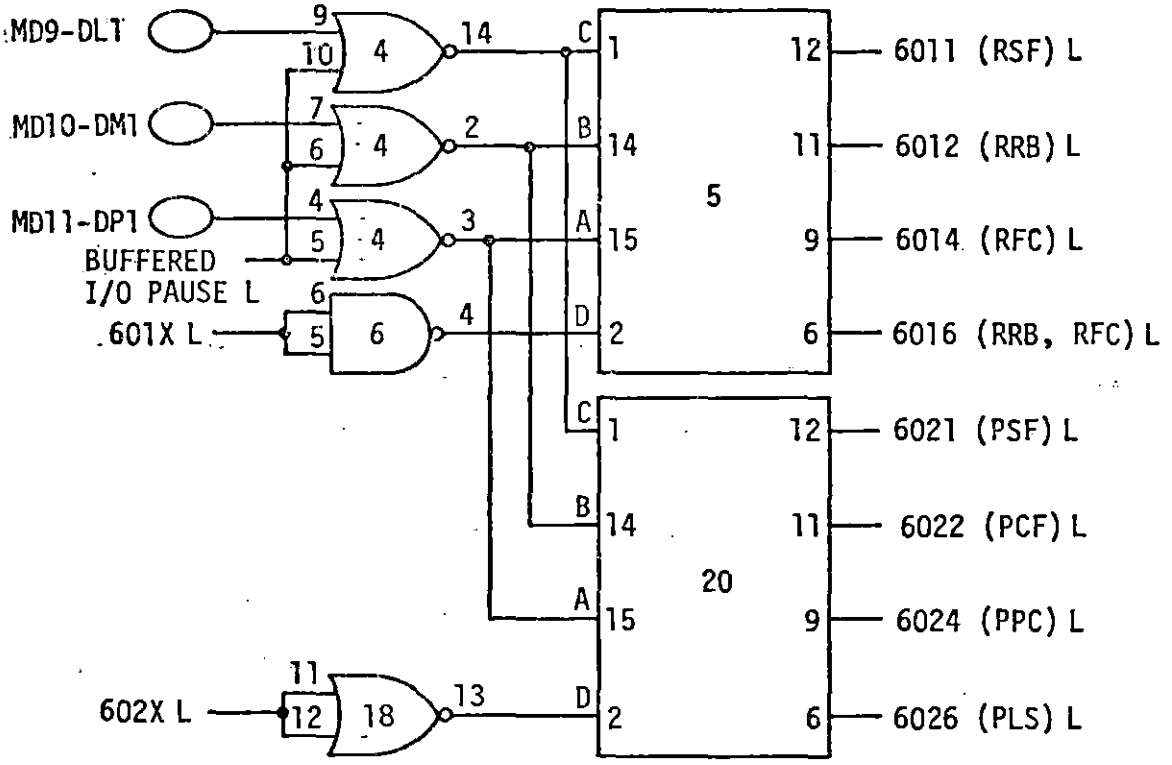


Figure 4. OPERATIONS DECODER Logic Diagram

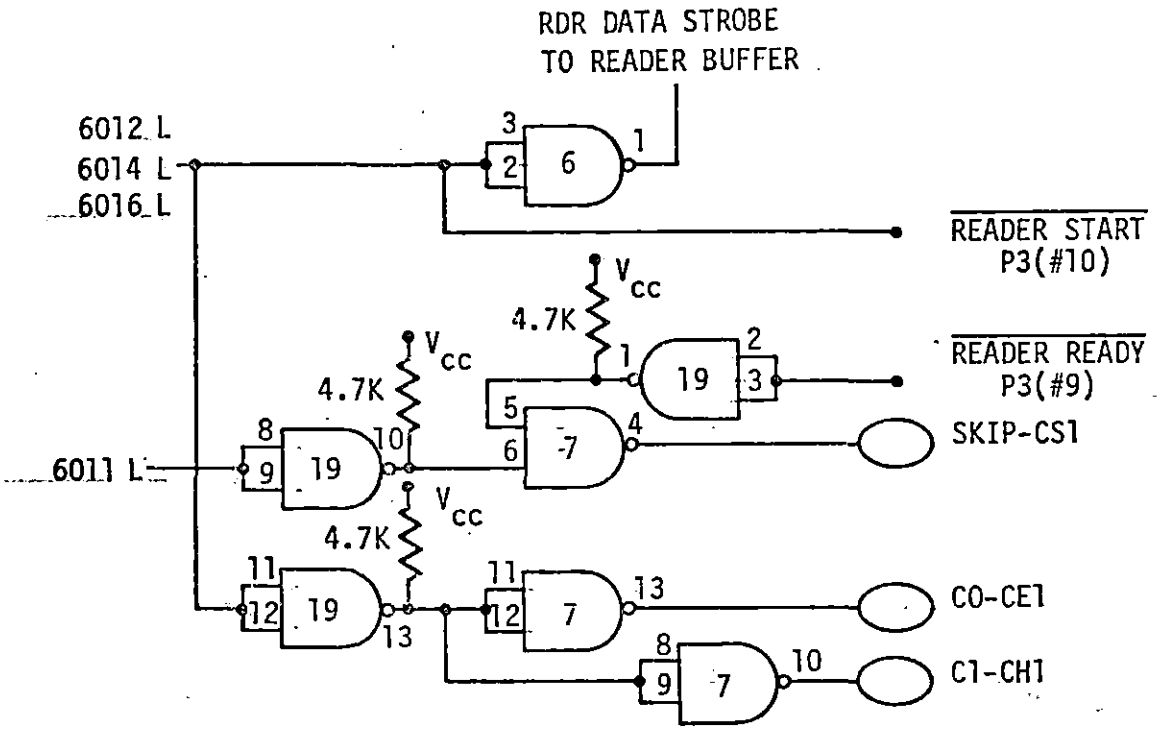


Figure 5. TAPE READ and SKIP Logic Diagram

Two important control signals, CO and C1 are used to determine the type of data transfer between the processor and the Heath control (2). When the data on READ HOLE 1-8 lines are passed through the READER BUFFER gates and put on the DATA BUS, the 6016 instruction asserts CO and C1, transferring the data to the Accumulator (AC) register.

Figure 6 is a timing diagram of the Heath Reader Handshake lines (6). Two handshake signals, $\overline{\text{READER START}}$ and $\overline{\text{READER READY}}$ are generated by the Heath Reader. The $\overline{\text{READER START}}$ signal (active low) advances tape one character. $\overline{\text{READER READY}}$ line (active low) is sensed by program instruction to determine when the data are ready to be transferred. $\overline{\text{READER START}}$ input may be pulsed only when this line is low.

TAPE PUNCH and SKIP Logic

The TAPE PUNCH and SKIP logic are shown in Figure 7. A tape loaded in the punch feeder mechanism can be punched, if a punch command is issued by an IOT instruction. When the 6026 IOT instruction is issued, for example, it applies a high-to-low transition to the $\overline{\text{PUNCH START}}$ line which initiates the punch cycle of a character. The 6021 instruction (Skip on Punch Flag) senses the state of the PUNCH READY line in the Skip logic. The PUNCH READY line being high indicates punch is ready. When this line is high, the program counter is incremented so that the next sequential instruction is skipped. Figure 8 is a timing diagram of the Heath punch handshake lines (6). Two handshake signals $\overline{\text{PUNCH START}}$ and PUNCH READY are generated by the Heath punch. The $\overline{\text{PUNCH START}}$ signal (active low) starts the punch cycle of a character. PUNCH READY (active high) indicates that the punch is ready. A TTL low is present from the Heath unit within

Table 2

IOT INSTRUCTIONS LIST AND DESCRIPTION[a]

Octal Code	Mnemonic	Function
6011	RSF	Skip on Reader Flag. Senses the state of the RDR FLAG flip-flop. If the flip-flop is set, the program counter is incremented so that the next sequential instruction is skipped.
6012	RRB	Read the RDR Buffer Register. Causes the RDR Buffer Register to be ORed into the AC Register, clears the RDR FLAG flip-flop.
6014	RFC	Fetch a Character from the tape. Clears the RDR FLAG flip-flop, loads a character into the RDR Buffer Register from the tape, sets the RDR FLAG flip-flop when the RDR Buffer Register is loaded.
6016	RRB, RFC	Microprogram of 6012 and 6014. RDR Buffer Register contents are ORed into AC Register, RDR FLAG flip-flop is cleared, character is loaded into Register, and RDR FLAG flip-flop is set.
6021	PSF	Skip on Punch Flag. Senses the state of the PUNCH FLAG flip-flop. If the flip-flop is set, the program counter is incremented so that the next sequential instruction is skipped.
6022	PCF	Clear the Flag. Clears the PUNCH FLAG flip-flop.
6024	PPC	Load Punch Buffer Register, Punch Character. Transfers the AC 4-11 contents to the Punch Buffer Register, punches the character, sets the PUNCH FLAG flip-flop when done.
6026	PLS	Microprogram of 6022 and 6024. Clears the PUNCH FLAG flip-flop, transfers AC 4-11 contents to the Punch Buffer Register, punches the character, sets the PUNCH FLAG flip-flop when done.

[a]Source: 7, p. 2-4.

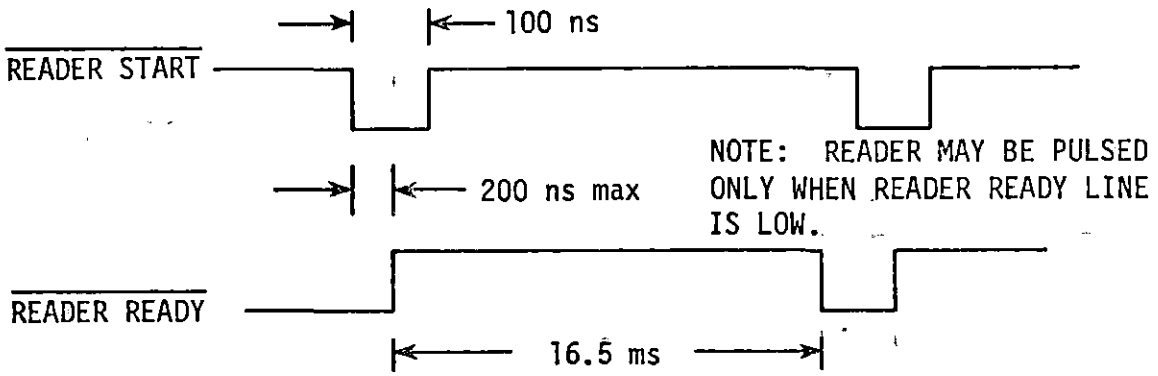


Figure 6. Timing Diagram for the Heath Reader Handshake Lines. Abstracted from (8).

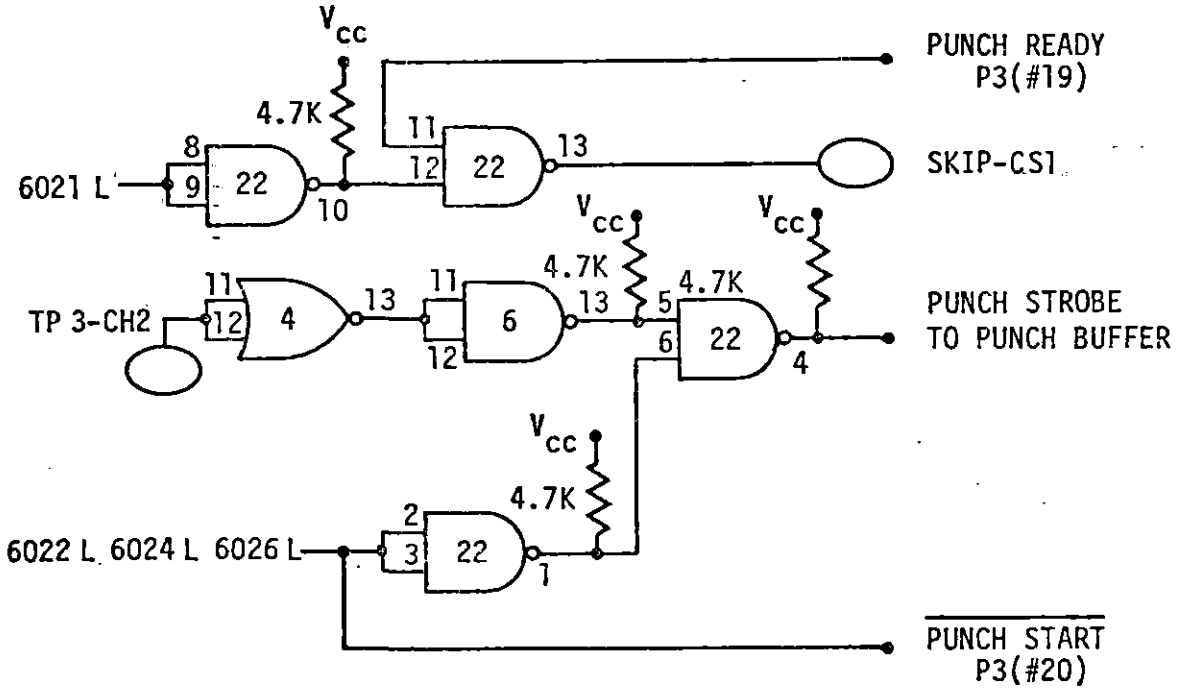
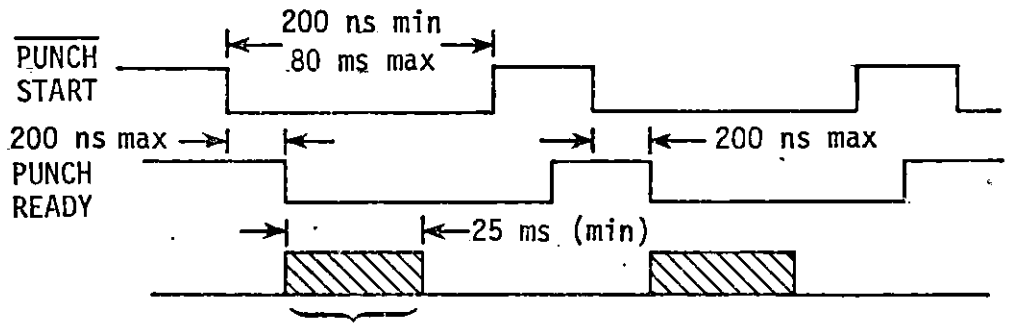


Figure 7. TAPE PUNCH and SKIP Logic Diagram



NOTE: PUNCH MAY BE TRIGGERED ONLY WHEN PUNCH READY LINE IS HIGH.

Figure 8. Timing Diagram for the Heath Punch Handshake Lines. Abstracted from (8).

200 ns after leading edge of $\overline{\text{PUNCH START}}$ input signal and remains low until the punch is ready for the next character.

READER BUFFER Logic

The READER BUFFER logic is shown in Figure 9. Data supplied on the READ HOLE 1-8 lines are enabled through the READER BUFFER gates in parallel form by the RDR DATA STROBE signal. Either the 6012, 6014 or 6016 instruction gates the character onto the OMNIBUS DATA 4-11 lines. At the same time, the IOT instruction asserts the OMNIBUS C0 and C1 signals, resulting in a transfer of the DATA 4-11 bits to the CPU AC register (5).

PUNCH BUFFER Logic

The PUNCH BUFFER logic is shown in Figure 10. It receives information from the AC via the DATA BUS, in parallel form, and transmits the information out to the Heath punch unit in parallel form.

A 602X instruction causes the loading of the DATA BUS (bits 4-11) into the PUNCH BUFFER registers (IC's 3 and 10). At Time TP3 of the 6022, 6024 or 6026 instruction, the PUNCH STROBE signal causes the transfer of the character signal from the PUNCH BUFFER registers to the PUNCH HOLE 1-8 lines. Information in the PUNCH BUFFER registers remain there until another punch instruction is issued (5). OMNIBUS signals C0 and C1 cause the transfer of the contents of the AC register to DATA BUS when pulled high.

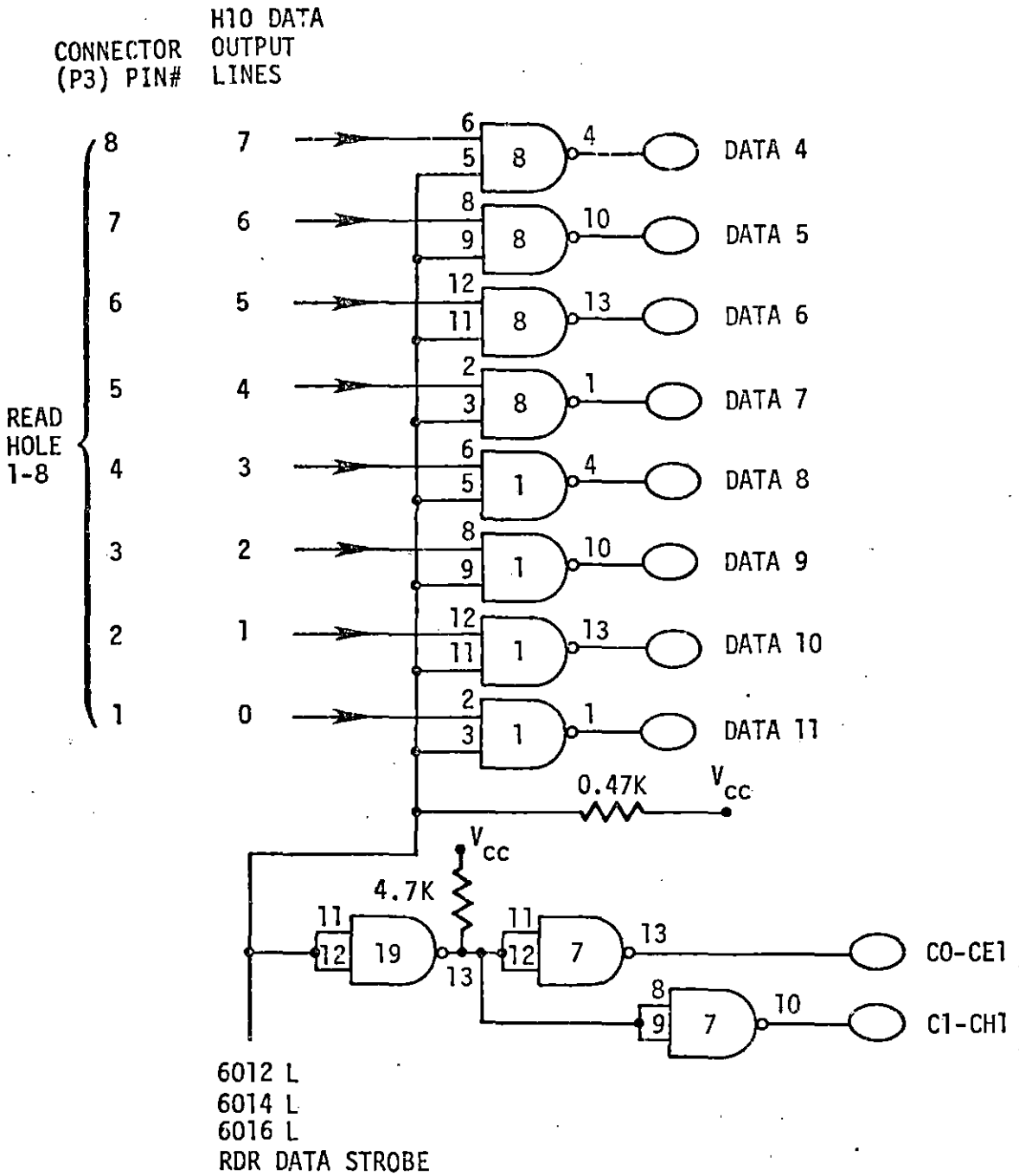


Figure 9. READER BUFFER Logic Diagram

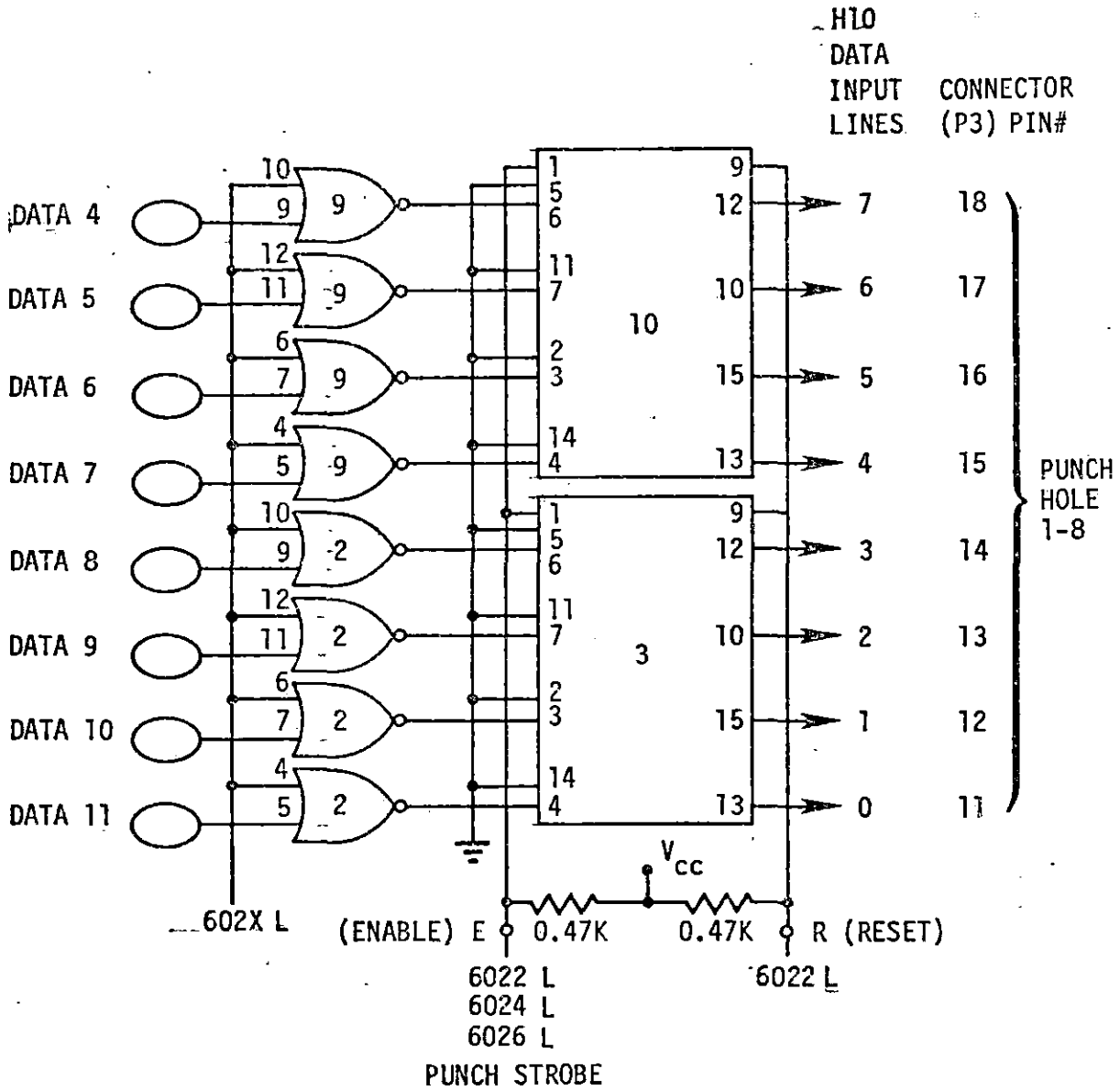


Figure 10. PUNCH BUFFER Logic Diagram

PHYSICAL DESCRIPTION

Printed Circuit (PC) Board

In order to interface to the PDP-8/E OMNIBUS, a printed circuit board of a special configuration is needed. This is available from Douglas Electronics (7). The board provides for both the special configuration adaptable to the PDP-8/E OMNIBUS and room for the mounting of integrated circuits (IC's) required for the interface.

For this interface, the mounting of IC's was done on a 26DE8 Douglas Electronics module which makes provision for some of the required chips. Mounting of additional IC's is required. Procurement of the Douglas board facilitated this interfacing design. The cost of this board is approximately $70. The inter-connecting of the IC's is done by soldering them on the Douglas board and hard-wiring them on the back to accomplish the desired functions (Figure 11). The physical layout of the mounted IC's on the module is shown in Figure 12. They are numbered 1 through 22 from left to right starting from the bottom row. The corresponding manufacturers IC numbers and their descriptions are listed in Table 1 (8,9).

Douglas boards are available with some of the IC's already mounted on them. In using these boards, however, certain modifications have to be made. In particular, since the use of interrupt in this interface design was not necessary, one must make certain that the interrupt request line (CP1) on the OMNIBUS is not affected (pulled low) when Douglas board is plugged into the OMNIBUS. Also, in most cases these boards are built to interface one peripheral unit only. However, the

Figure 11. Hand-wired inter-connection of the IC's on the back of the Douglas Board

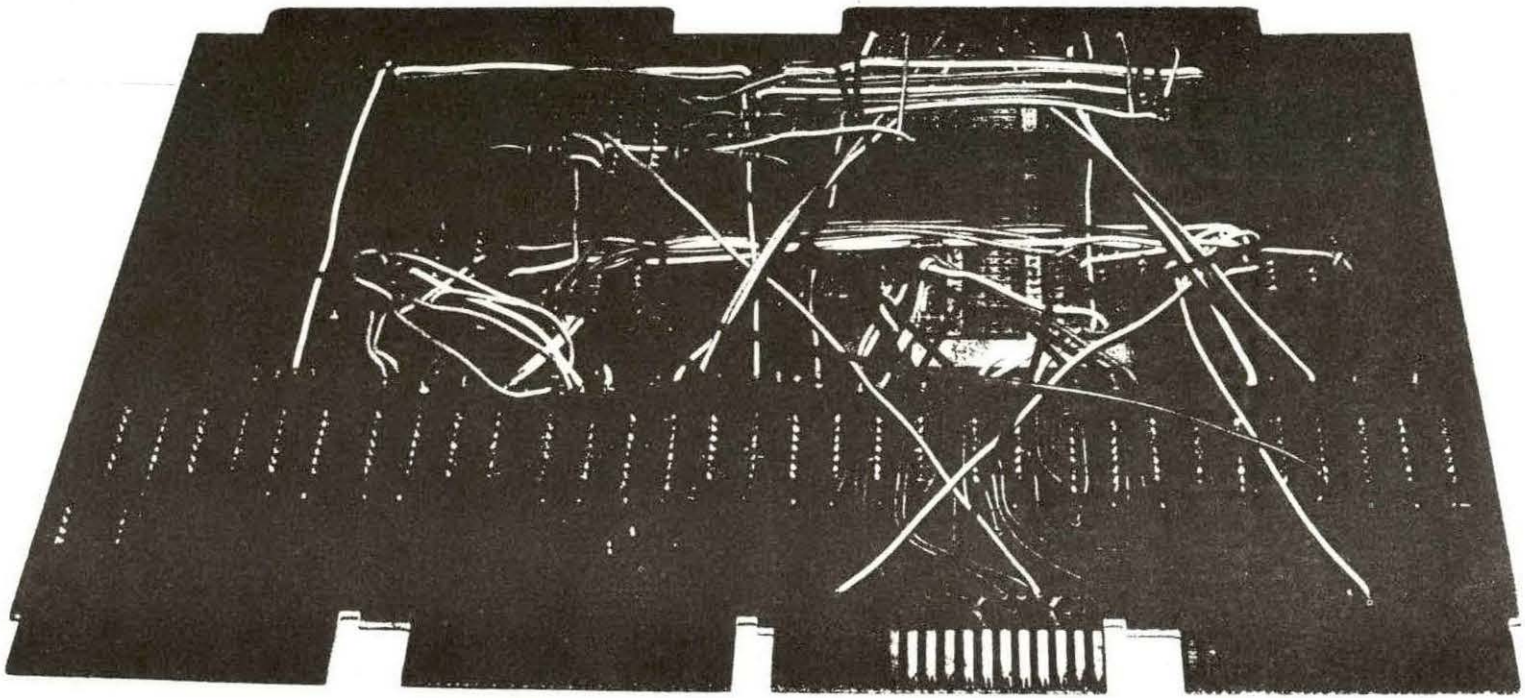
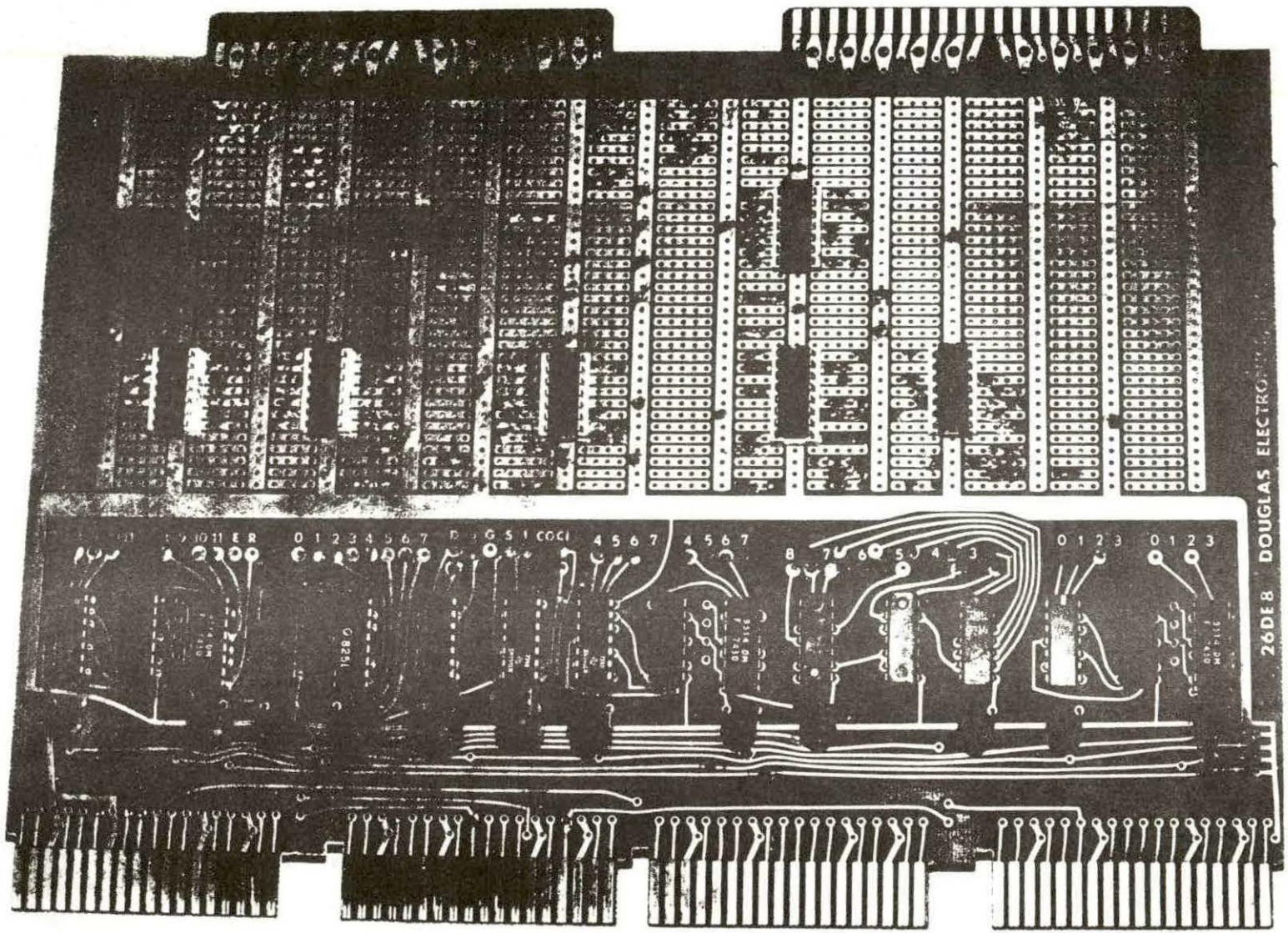


Figure 12. Physical layout of the mounted IC's on the Douglas Board


26DE8
DOUGLAS ELECTRO

Heath unit functions as two separate peripheral units and must be addressed with two different codes, i.e., one for the reader and one for the punch. Thus in using the Douglas board, three of the printed lines have to be physically disconnected and rerouted to allow for both the reader and the punch logic. The three lines which connect IC's 2, 9 and 15 (on the Douglas board) to pin 2 of IC 5 should be disconnected and rerouted to pin 2 of IC 20.

The interface control module plugs into the PDP-8/E OMNIBUS and connects to the external Heath reader/punch through a single cable. See Figures 13 and 14.

Signal Cable

The signal cable is a 10-foot-long, 25-conductor cable with three of the conductors not used. See Figures 15 and 16. Table 3 lists the Cable/Connector pin assignments.

Heath Reader/Punch

The paper tape reader/punch is a Heath model H10, manufactured by Heath Company (10). It weighs about 22 pounds (10 kgs) and its overall dimensions are:

9-3/4"S x 10-5/8"W x 12-5/8"H (24.77 Cm W x 49.85 Cm D x 32 Cm H)

Power requirements: 100-135 volts or 200-270 volts,
50-60 HZ, 100 watts maximum.

The Heath reader/punch reads and punches standard 8-level, 1-inch (10-inch maximum diameter roll or fan-fold), oiled or unoiled paper tape. It has a maximum reading speed of 50 characters per second and a maximum punching speed of 10 characters per second. A picture is shown in Figure 17.

Figure 13. Heath unit, interface board and the cable connected together

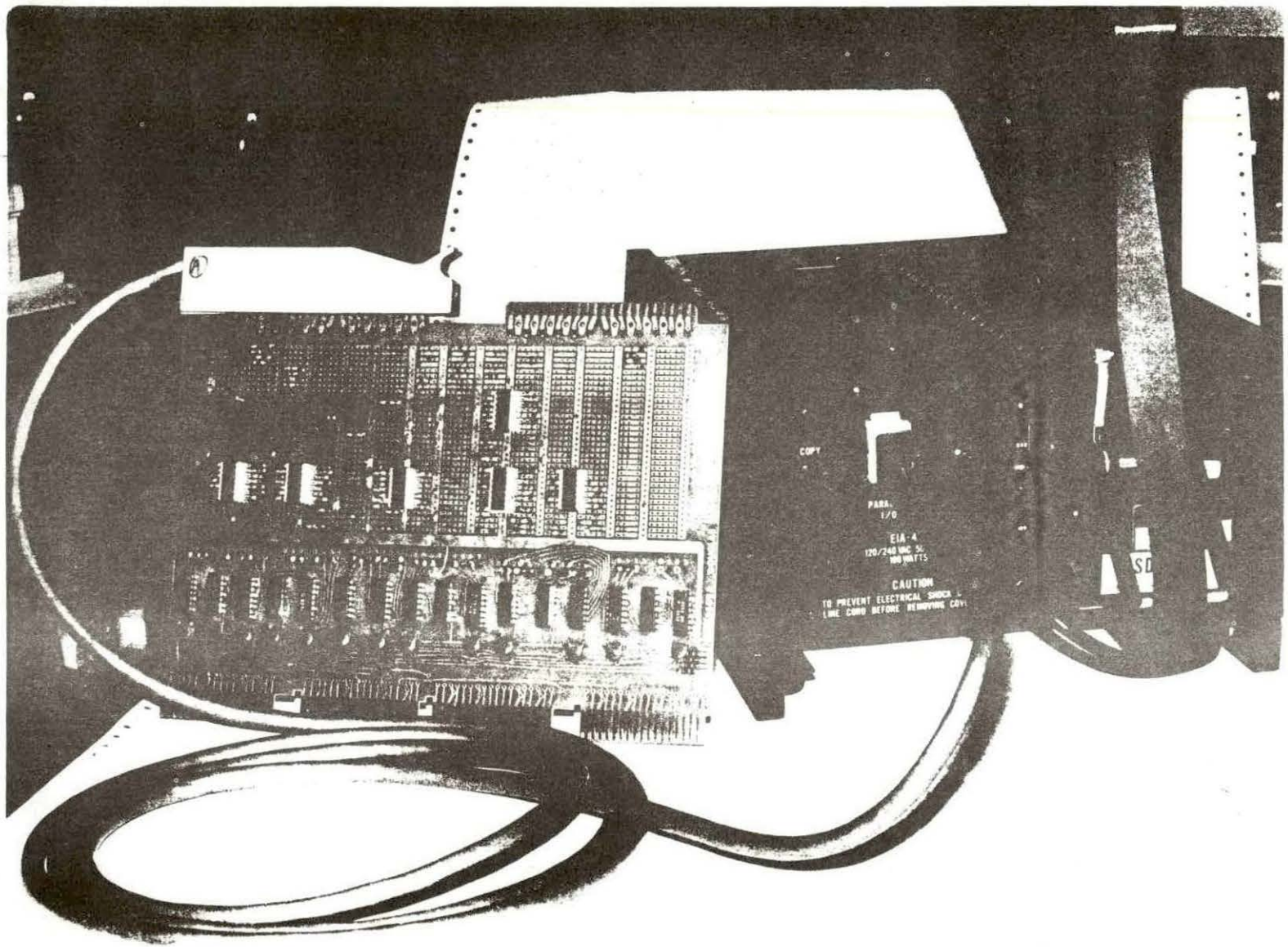
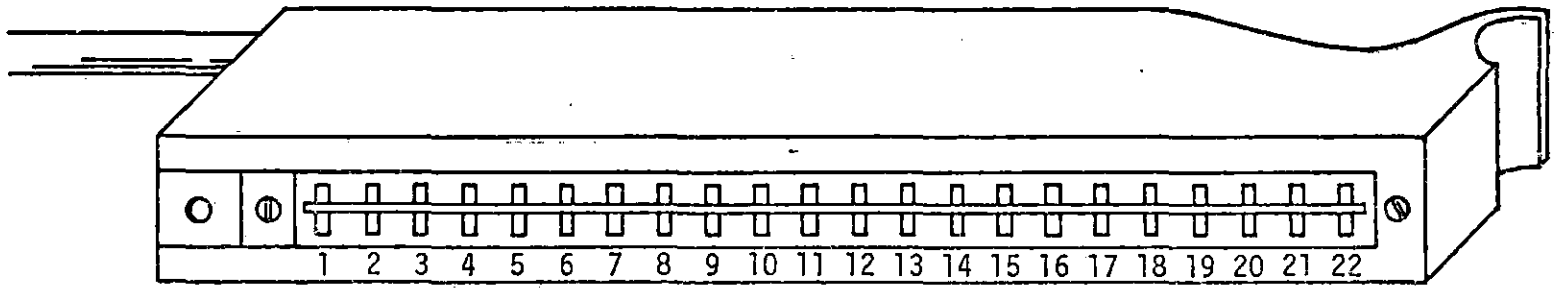

COPY
PARA.
I/O
EIA-4
CAUTION

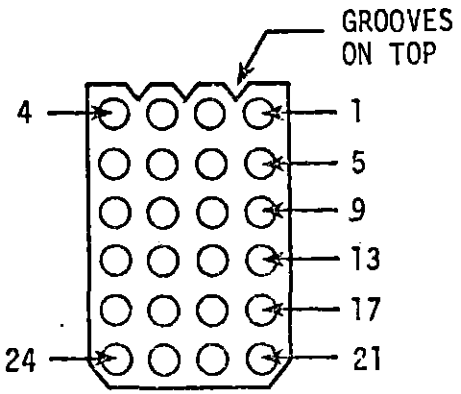
Figure 14. Heath unit, interface board and the cable connected together with the interface control module inserted in the OMNIBUS

Figure 15. Signal cable

Figure 16. Pin connection numbering of sides A and B of the signal cable



HOOD BOTTOM VIEW



P3 FEMALE CONNECTOR
VIEWED FROM OUTSIDE
OF REAR PANEL

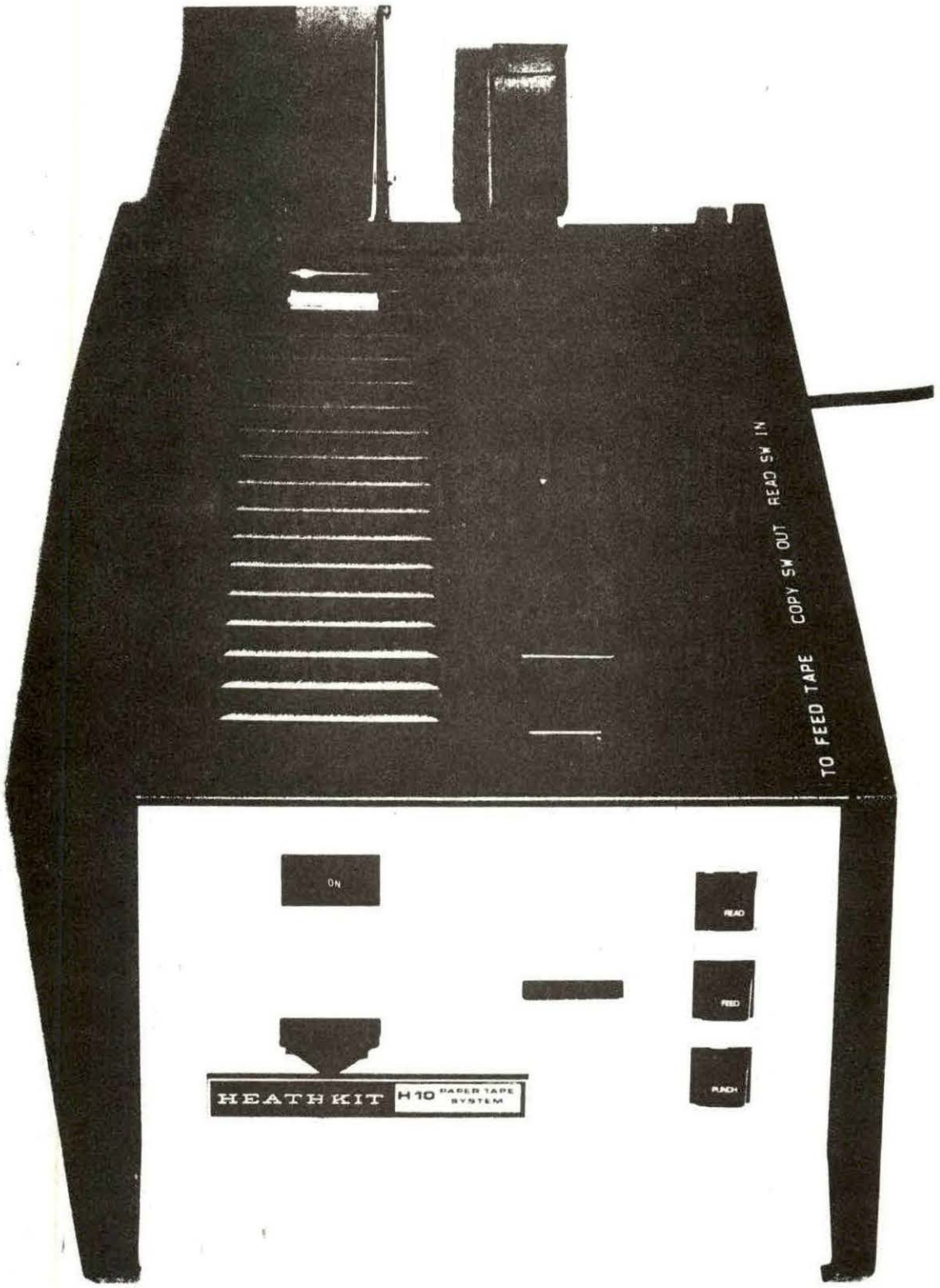
Table 3

CABLE/CONNECTOR PIN ASSIGNMENTS

Hood Pin # (Side A)	Connector (P3) Pin # (Side B)	Wire Color	Signal Name
1	1	RED	READ HOLE Line 1
2	2	WHT-BLK-RED	READ HOLE Line 2
3	3	ORG-GRN	READ HOLE Line 3
4	4	BLK-WHT	READ HOLE Line 4
5	5	WHT	READ HOLE Line 5
6	6	GRN	READ HOLE Line 6
7	7	ORG-RED	READ HOLE Line 7
8	8	BLU-RED	READ HOLE Line 8
9	9	BLK-BRN	$\overline{\text{READER READY}}$
10	10	BLU-WHT	$\overline{\text{READER START}}$
11	11	RED-GRN	PUNCH HOLE Line 1
12	12	BLU-BLK	PUNCH HOLE Line 2
13	13	ORG-BLK	PUNCH HOLE Line 3
14	14	GRN-WHT	PUNCH HOLE Line 4
15	15	WHT-BLK	PUNCH HOLE Line 5
16	16	WHT-RED	PUNCH HOLE Line 6
17	17	GRN-BLK	PUNCH HOLE Line 7
18	18	BLU	PUNCH HOLE Line 8
19	19	RED-BLK	PUNCH READY
20	20	RED-WHT	$\overline{\text{PUNCH START}}$
21	21	ORG	$\overline{\text{PUNCH READY}}$
--	22	N.C.[a]	
--	23	N.C.[a]	
22	24	BLK	GROUND

[a] N.C.: No connection.

Figure 17. Heath model H10 paper tape reader/punch


TO FEED TAPE COPY SW OUT READ SW IN
ON
READ
FEED
PUNCH
HEATH KIT H10 PAPER TAPE SYSTEM

INSTALLATION

The interface control module is inserted in the PDP-8/E OMNIBUS. The control module is connected to the Heath reader/punch with the signal cable. The hood side of the cable (side A) connects to the control module and the female connector side of the cable (side B) plugs into the male connector (P3) on the back of the Heath unit. Refer to Figure 14.

BASIC COMPUTER OPERATION

In order for the Heath high-speed paper tape reader/punch to communicate with the PDP-8/E minicomputer, there must exist an active device handler program in the existing operating system (OS/8). The Heath interface control board is designed so that it operates under the control of the device handler for the DEC high-speed paper tape reader/punch. This device handler is supplied with the system generation program for OS/8, (BUILD). Only one of the device handlers, either the low-speed reader/punch (Teletype handler) or the DEC high-speed reader/punch handler can be active at one time. To make the desired device handler active, the BUILD commands DELETE and INSERT are used (3). This procedure is shown below.

The following command is typed in response to the dot printed by the OS/8 Keyboard Monitor.

RUN SYS BUILD

BUILD responds by printing a $, signaling that it is ready to accept commands. Typing the following commands, respectively, deactivates the existing paper tape reader/punch handler and activates the high-speed paper tape reader/punch handler.

DELETE PTR

DELETE PTP

INSERT PT8E PTR

INSERT PT8E PTP

BOOTSTRAP

OS/8 then prints the following two lines and a dot indicating that

the control is returned to the Keyboard Monitor.

DSK = SYS

SYS BUILD

.

To preserve the current system status the following is typed in response to the dot printed by the Keyboard Monitor:

SAVE SYS BUILD

To deactivate the high-speed reader/punch handler and activate the Teletype handler, the previous procedure is repeated with the following exception:

The commands INSERT PT8E PTR and INSERT PT8E PTP are replaced with INSERT KS33 PTR and INSERT KS33 PTP.

Loading of Binary Programs

After the high-speed paper tape reader/punch handler has been activated using BUILD, binary programs on tapes can be loaded and run via the Heath reader. This is done using the Absolute Loader (ABSLDR). The user calls the ABSLDR from the system device by typing the following in response to the dot printed by the Keyboard Monitor (3):

R ABSLDR

The system prints an asterisk (*) when it is ready to receive a command line. The following command is typed in response to the asterisk:

PTR:/G

The command decoder responds by printing an up-arrow (↑) or (^). At this point the program on paper tape is inserted in the reader and the READ switch located on the Heath front panel is turned on (IN position).

Typing any character on the keyboard causes the tape to be read. After the tape is fed through completely, the reader stops automatically. The outcome of the program on the tape will be printed on the Teleprinter and the computer halts. At this point the program loaded may not be physically in core (3). To examine core locations after using ABSLDR, use Octal Debugging Technique (ODT). Running the program under ODT ensures the loading of the information in core. The same program can be run again by hitting the CONTINUE switch on the PDP-8/E front panel. To get back to the Monitor, the procedure for bootstrapping the OS/8 System must be performed.

Punching of Binary Programs

Information contained in selected blocks of core memory can be punched on the Heath punch as binary-coded paper tape using the Binary Punch program (11). This program is loaded by means of the Binary Loader (2). It basically picks up data from memory and punches it on paper tape via high-speed or Teletype Punch.

This procedure is used when, there are only a DEC PDP-8/E, a Decwriter and the Heath paper tape reader/punch available to the user. When a DECtape transport is available, storing and punching of binary programs on paper tape can be accomplished much easier. Information can be stored on and recalled from the magnetic tape rather than the PDP-8/E core memory. The explanation of this procedure follows.

Data Transfer Between Magnetic and Paper Tapes

Reading

To store a binary tape on the DECtape transport via Heath paper tape reader, the Peripheral Interchange Program (PIP) is used.

To call PIP from the system device, in response to the dot printed by the Keyboard Monitor, the user types:

R PIP

The command decoder then prints an asterisk (*) at the left margin of the Teleprinter paper and waits to receive a line of I/O files and options (3). The following is typed in response to the asterisk:

DTAO: File name<PTR:/B

The command decoder responds by printing an up-arrow (↑) or (^). At this point the tape is inserted under the reader head and the READ switch is turned on (IN position). Finally, typing any character on the keyboard causes the information to be transferred to the magnetic tape. After the paper tape is fed through completely, the READ switch is turned off (OUT position).

Punching

To punch a binary tape on the Heath paper tape punch from DECtape transport, the procedure below if followed:

R PIP

The Heath PUNCH switch is turned on (IN position). (Note: The READ switch will not affect the punch operation). The following command is then typed in response to the asterisk (*).

PTP:<DTAO: File name/B

The PUNCH switch stays on during the entire punch operation.

After the tape punch is completed, the system returns to PIP automatically.

CONCLUSION

A digital electronic interface was designed to enable a Digital Equipment Corporation PDP-8/E minicomputer to exchange data with a Heath model H10 paper tape reader/punch. The design was implemented with TTL integrated circuitry. It has been tested in the laboratory and performs satisfactorily.

With the Heath unit now installed, data can be transferred to the core memory of the PDP-8/E at a maximum speed of 50 characters per second (6). Also, the Heath interface permits recording of any data or program on paper tape for long-term storage.

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APPENDIX

OMNIBUS Signals

The signals and pin assignments of the OMNIBUS were abstracted from Reference 2 and are given in Figure 18. The L and H after the signal name identifies the most common assertion level. The description of each signal in the interface logic is provided in Table 4.

TABLE 4

Programmed I/O OMNIBUS Signals

Abstracted from (2)

SIGNAL	FUNCTION
MD 0-11 L	Provides IOT instruction as follows: 6_8 (used by processor) (0 1 2) — Device Select Code (3 4 5 6 7 8) — Device Operation Code (9 10 11)
I/O PAUSE L	Used to gate the device select and device operation codes into the programmed I/O interface decoders and generate BUS STROBE at TP 3. I/O PAUSE is grounded when MD 0-2 equals 6 (octal).
TP 3 H	TP 3 is used to clear the flag and clock the output buffer of a Programmed I/O interface. It is generated in the timing generator as a positive-going 100 ns pulse.
INTERNAL I/O L	Signal INTERNAL I/O is grounded by the device selector decoder. The Positive I/O Bus Interface cannot generate IOP's when this line is grounded. This inhibits decoding any Internal OMNIBUS IOT

TABLE 4 (Continued)

SIGNAL	FUNCTION
	instruction. Failure to ground this line will result in long IOT timing.
DATA 4-11 L	The 8 DATA lines called DATA BUS serves as a bidirectional bus for both input and output data, between the AC register in the processor and the interface buffer register. During Time State TS 3 of an IOT instruction, the contents of the DATA BUS are applied to the processor's major register gating in accordance with the C lines. For output transfers, information must be taken from the DATA BUS by edge triggering only, using the leading edge of TP 3.
C lines: C0, C1 L	Signals C0 and C1 determine the type of transfer between a device and the processor. These lines control the data path within the processor and determine if data are to be placed onto the DATA BUS (C0 and C1 high) or received from the DATA BUS (C0 and C1 low).
SKIP L	An IOT checks the flag for a ONE state and causes the device logic to ground the SKIP line if the flag is set. The result (PC + 1) is loaded into Central Processor Memory Address Register (CPMA). The SKIP line is sampled by the processor at TP 3, and must be grounded 50 ns before TP 3 in order for the skip to occur.

Figure 18. Signals and pin assignments of the OMNIBUS

PIN	D1	D2	C1	C2	B1	B2	A1	A2
A	TP	+15V	TP	+5V	TP	+5V	TP	+5V
B	TP	−15V	TP	−15	TP	−15V	TP	−15V
C	GND	GND	GND	GND	GND	GND	SP GND *	GND
D	MA8L	IR0L	I/O PAUSE L	TP1H	MA4L	INT STROBE H	MA0 L	EMA0L
E	MA9L	IR1L	C0L	TP2H	MA5L	BRK IN PROG L I	MA1L	EMA1L
F	GND	GND	GND	GND	GND	GND	GND	GND
H	MA10L	IR2 L	C1L	TP3H	MA6L	MA,MS LOAD CONT L	MA2L	EMA2 L
J	MA11L	FL	C2 L	TP4H	MA7L	OVERFLOW L	MA3 L	MEM START L
K	MD8L	DL	BUS STROBE L	TS1 L	MD4 L	BREAK DATA CONT L	MD0 L	MD DIR L
L	MD9L	EL	INTERNAL I/O L	TS2 L	MD5 L	BREAK CYCLE L	MD1L	SOURCE H
M	MD10L	USER MODE H	NOT LAST XFER L	TS3 L	MD6 L	LA ENABLE L	MD2 L	STROBE H
N	GND	GND	GND	GND	GND	GND	GND	GND
P	MD11L	F SET L	INT ROST L	TS4 L	MD7 L	INT IN PROG H	MD3 L	INHIBIT H
R	DATA 8 L	PULSE LA H	INITIALIZE H	LINK DATA L	DATA 4 L	RES 1 H	DATA 0 L	RETURN H
S	DATA 9 L	STOP L	SKIP L	LINK LOAD L	DATA 5 L	RES 2 H.	DATA 1 L	WRITE H
T	GND	GND	GND	GND	GND	GND	GND	GND
U	DATA 10 L	KEY CONTROL L	CPMA DISABLE L	IND 1 L	DATA 6 L	RUN L	DATA 2 L	ROM ADDRESS L
V	DATA 11 L	SW	MS,IR DISABLE L	IND2 L	DATA 7 L	POWER OK H	DATA 3 L	LINK L

* THIS PIN IS CONNECTED TO GROUND ON THE BUS, BUT SERVES AS A LOGIC SIGNAL WITHIN MODULES TO FACILITATE TESTING.